Numerical models of MOS devices and modelling methodology of physical effects in IC substrates.

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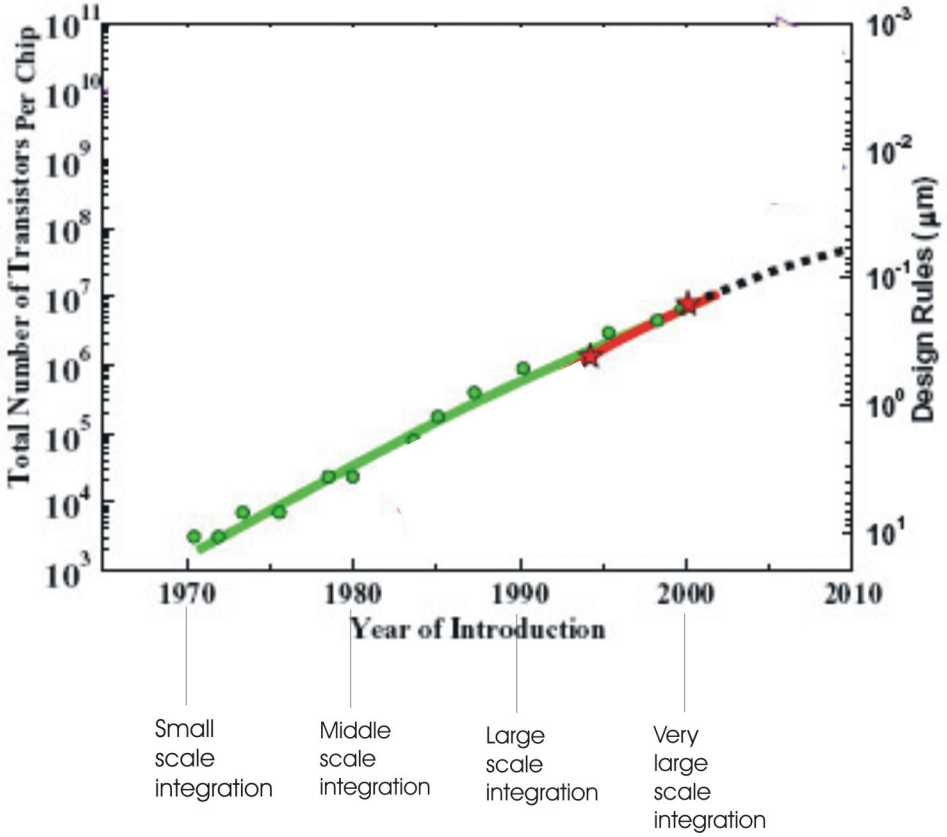
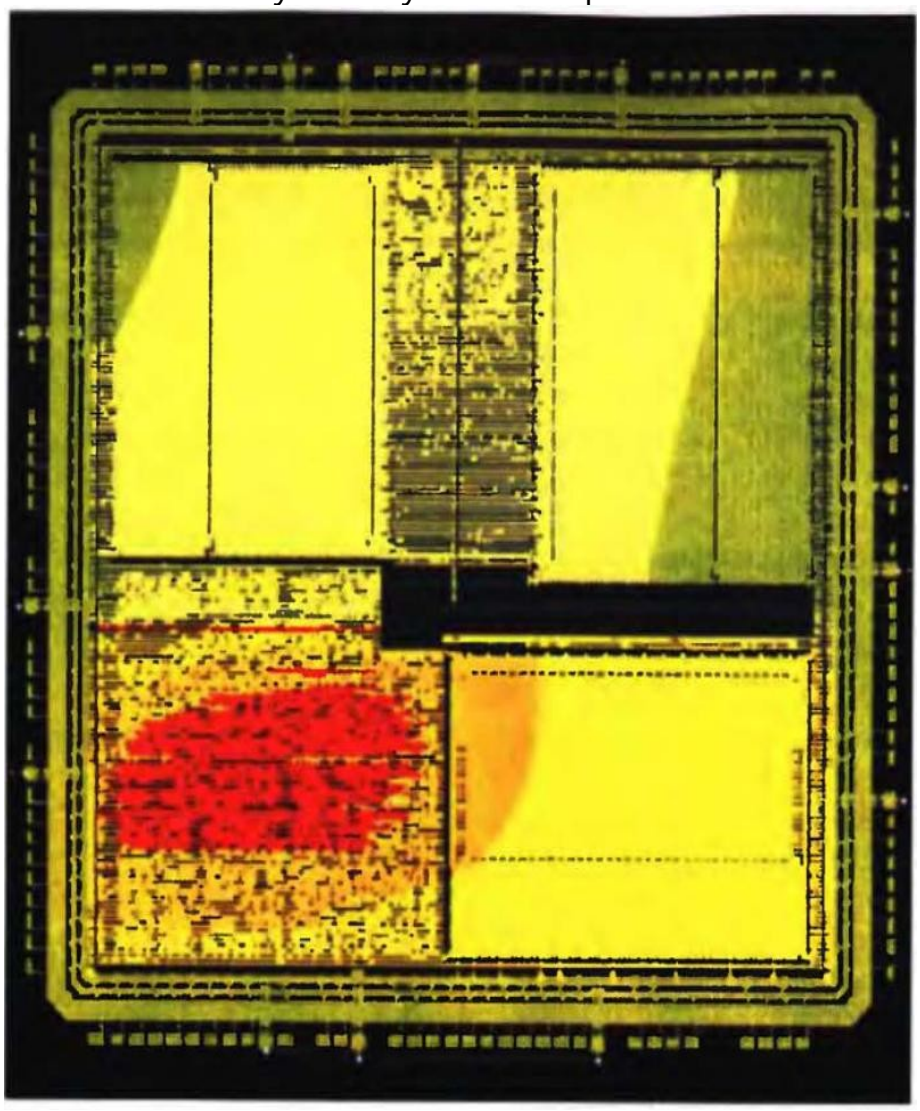
The understanding, prediction and control of new and not-researched interactions in integrated circuits has been a major research goal in development of analog, mixed-signal and high-performance digital integrated circuits since the birth of semiconductor industry in 1960s. The most important of these is thermal effects and electrical interactions through the substrate. Since the physical origin of these was often not well understood, characterized and modeled, the interactions were often not evident until actual devices were fabricated, requiring several re-design cycles. This problem especially severe in the complexity of mixed-signal circuits that have high operating frequencies and wide bandwidth.
The semiconductor industry today is moving towards an area in which analog and digital IP-blocks will place together on large complex chips, resulting in far higher levels of integration.



Thus unforeseen interactions between integrated devices should be more effectively predicted during design process. Alike we can see very greater miniaturization and increase of device density on the chips. As well to support the latest technologies in semiconductor fabrication, the last 5 or 7 years we have seen a continuous restructuring of design practices. IC development flows are moving to 'System-on-chip' projects. There are new IC design methodologies are coming and development and applying of new effective approachies to

system-on-chip design is a mainstream today in the semiconductor industry when 'substrate noise' problem is one of the important. Today research in substrate noise is focused on the miltylayer substrate characterization.
Substrate noise was a constant and dominant impact in the design of analog and mixed-signal integrated circuits. Due to substrate noise can covers all chip, IC designer can see performance changes of most components, especially in analog part, thus resulting in partial or total decrease of functionality in the system-on-chip.



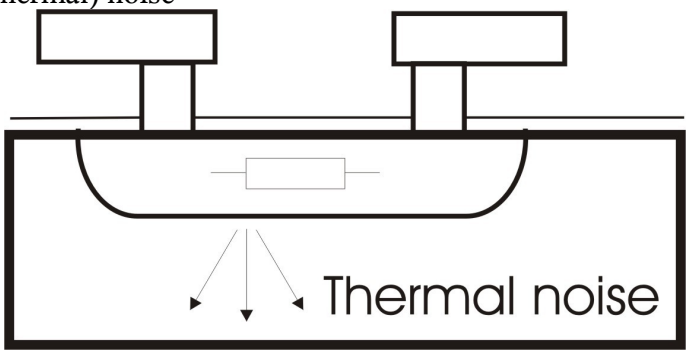
During last 5 years, we can see very fast semiconductor chips miniaturazation, applying new paradigms new features in integrated circuits design:

- Complexity and integration level are increase with moving to new technology generation
- IC development flows are moving to 'System-on-chip' projects
- Deep submicron technology process are using. New physics effects are incoming
- Impact from effects in IC substrate are increasing

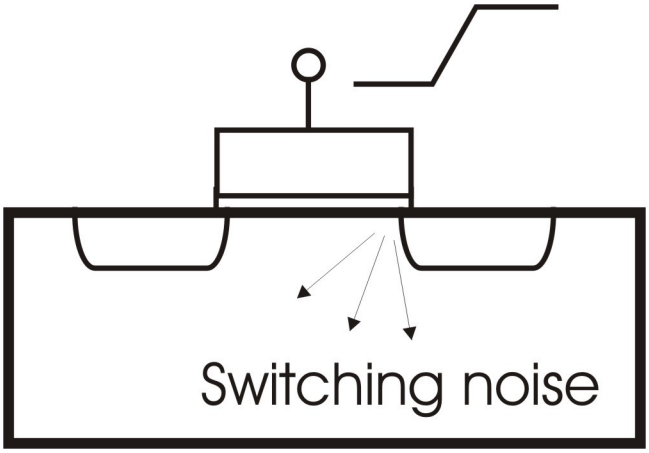
Noise in substrate begin impact in the digital part of the chips. And today definitely we can say that digital circuits very sensitive from this effects, and since the resulting threshold voltage modulation dynamically changes gate delays locally, thus impacting in the performance of all system that are difficult to predict.

Substrate noise can be classified on the following sections:

- intrinsic (thermal) noise



- switching noise



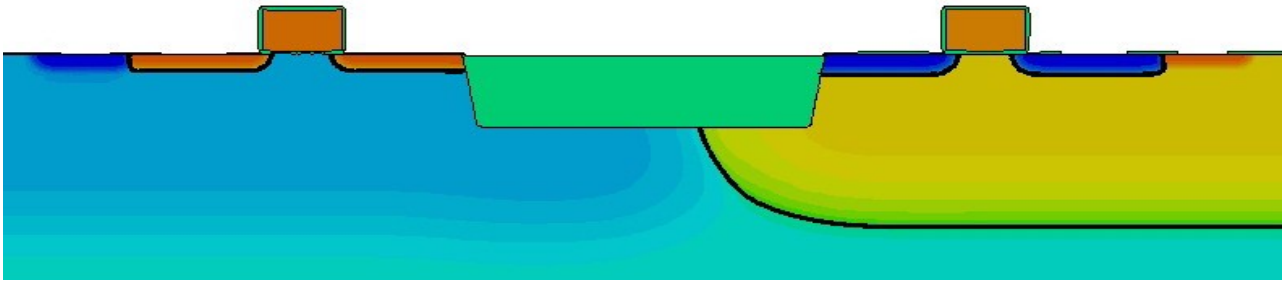
Intrinsic noise – is a thermal noise that occurs by circuit signals on the resistive components. The power of this noise very small compared with switching noise. Thus, intrinsic noise often ignored in most of the software tools for substrate noise analysis.
Switching noise – is noise that births in digital blocks during fast switching of MOS transistors and occurs in drain regions. During MOS devices switching current pulses inject in to the substrate and this interacts can distribute through substrate body on difference depth and on difference distance and can be detected by sensitive circuits. The path of distribution of this noise is depend on disposition of the noise sources, circuits contacts, doping profile and substrate potential. As well we need to know that accurate modeling of substrate noise requires several techniques to model switching noise injection, transport and reception mechanisms.
Technology CAD systems are very often use in system-on-chip design today. TCAD helps solve the following problems:

- Development of technology processes and integrated device constructions
- Definition of the minimal layout size and library cell creation
- Calculation of effects in SoC substrate that define interaction between integrated devices
- Calculation of electrophysical parameters, electrical characteristics of integrated devices using numerical multidimentional modelling of IC blocks and substrate cross sections

Process engineers can develop and optimize new technology processes and device constructions. Layout designers can define minimal design rules and compile standart cell libraries. Technology CAD systems allow visualize physical effects in system-on-chip substrate thus help IC designers define interactions between integrated devices, calculate

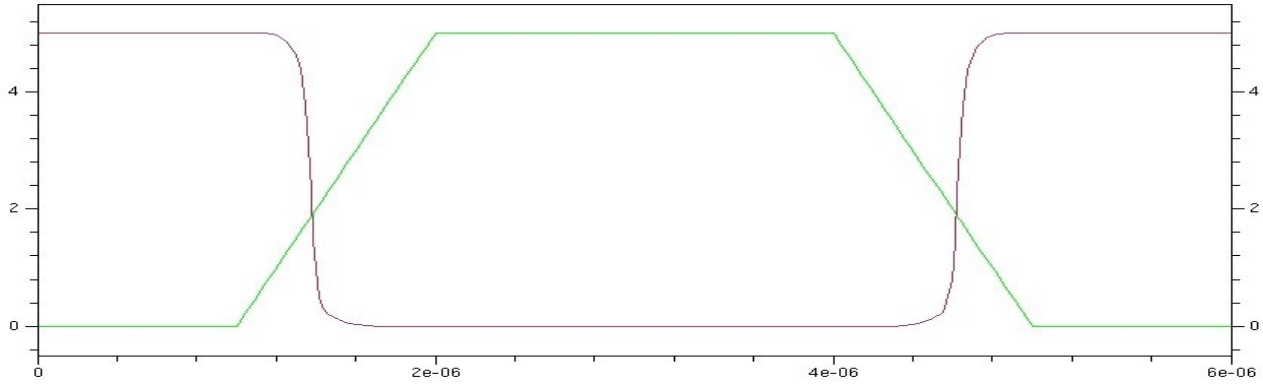
electro-physical parameters and electrical characteristics of integrated structures.

In this work we performed transient analysis of CMOS structure with STI isolation.

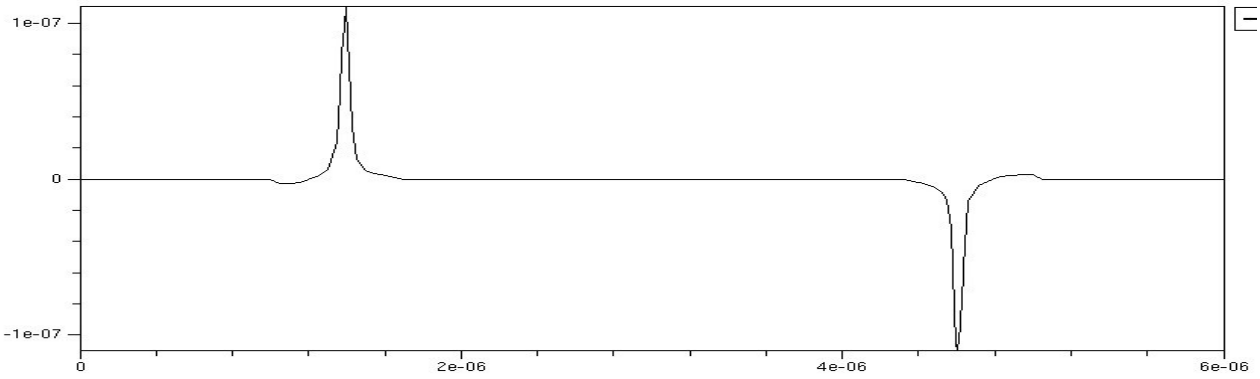


The modeling was performed using SDevices tool from TCAD Synopsys CAD package. We have researched effects in substrate during CMOS-gate switching. There is input and output signals and current through substrate.

- Input and output pulse signals



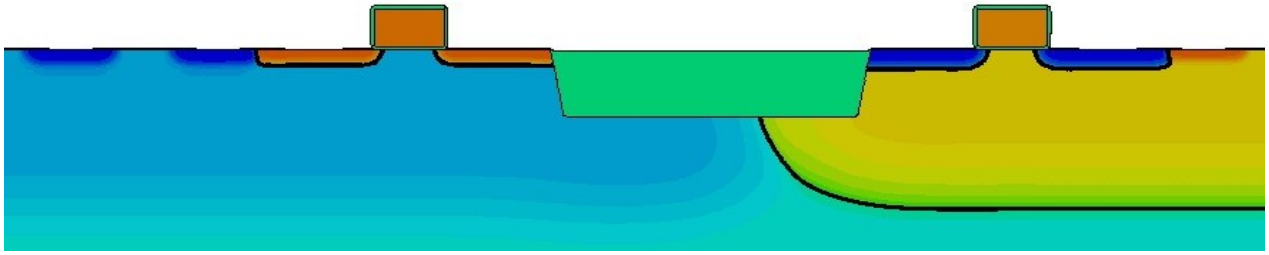
- Dynamic current change through substrate contact



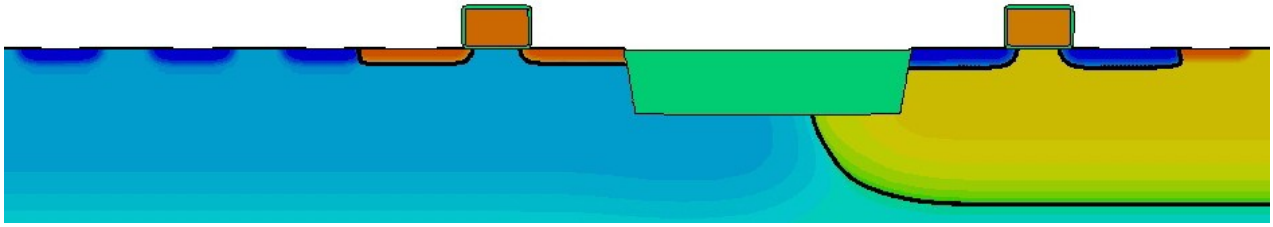
As was expected, we see current injection during switch process and fluctuation in current through substrate contact.

Substrate current distribution can be analysed using structures with distributed substrate contacts (2 and 3 contacts).

- CMOS cross section with 2 substrate contacts

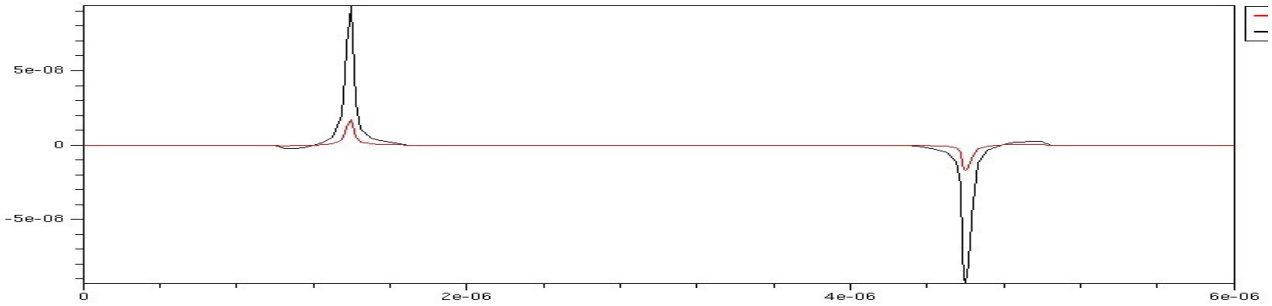


- CMOS cross section with 3 substrate contacts

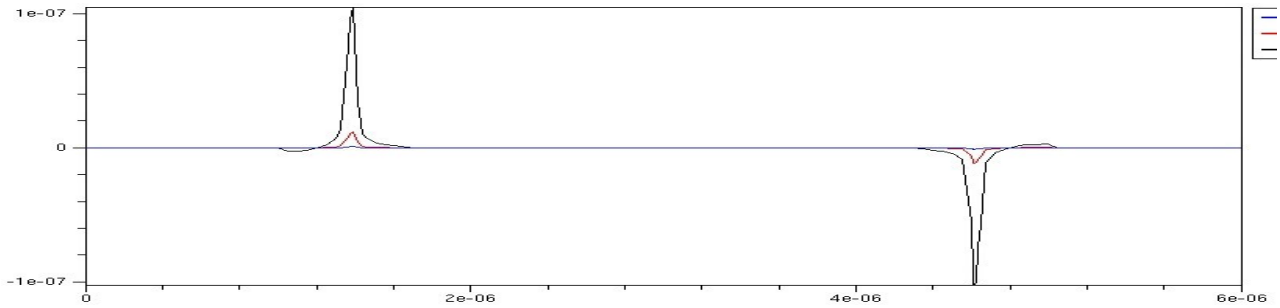


There is currents through 2 and 3 substrate contacts

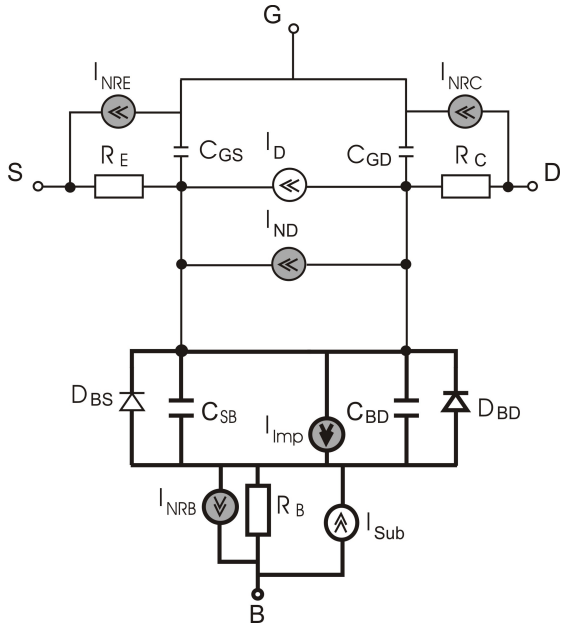
- Substrate current injection in structure with 2 contacts



- Substrate current injection in structure with 3 contacts



Based on the results of device modeling we've modified equivalent electrical circuits by adding elements that shows interaction between MOS structure and substrate.

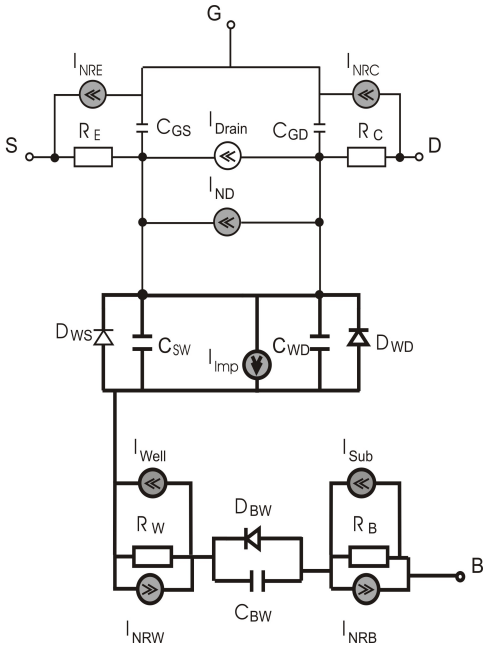


N-MOS transistor interacts directly with substrate through source-bulk and drain-bulk capacitances. On this equivalent circuits elements Cdb and Csb are modelling capacitances of the source-bulk and drain-bulk junctions. Dark sources are modeling noise sources of the diffusion regions. But more interested to see on the 2 elements that added in to equivalent circuits. This is:

Isub – element that models space charge impact on the channel current (receptor).

And Iimp – element that models current, generated with impact ionization physical effect near drain region during switching of the CMOS structure. This source most affect to the current through the substrate contacts.

The similar situation we see during research pMOS transistor in N-well, but current injection mechanism in this case is more complex die to N_well-Bulk junction.



P-MOS transistor interacts with substrate similarly as n-MOS. As well p_mos has current injection sources and sources that modeling p-mos interaction with substrate.

Resume:
We have developed methodology of modeling of integrated elements through substrate including functional layers formation using technology process modeling, calculation of electrical characteristic and charge distribution in substrate, analysis of MOS transistors parameters and dynamic of change distribution in substrate. We have modified nonlinear equivalent circuits for p- and n-MOS devices by adding elements that taking into account substrate coupling.
We have performed technology and device simulation of p- and n-MOS devices in digital gate with one and several distributed substrate contacts. We have research properties of MOS-transistors as sources and receptors of noise distributed in substrate.