Statistical Static-Timing Analysis: From Basic Principles to State of the Art [1]

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Abstract

The following report introduces the notion of Statistical Static Timing Analysis and the reasons for its ongrowing necessity in current and future integrated circuit manufacturing. This paper is based on a presentation conducted during the Moscow-Bavarian Joint Advanced Student School in March 2009. Therefore, it serves as an extention to the slides by providing more thorough explanation to them. The matter considered in this writing gradually increases in complexity. Starting with the idea and basic concepts of modelling delay in statistical fashion, the subject is then extended into applying these concepts in delay propagation and calculation in integrated circuit analysis.

Contents

1 Introduction

1.1 What is Static-Timing Analysis?

Let us first introduce the notion of Static-Timing Analysis (STA) in order to grasp its significance in today's integrated circuit design and manufacturing.

STA is a tool, which is widely used to determine the delay of integrated digital circuits. In order to have a properly operating circuit, not only the design needs to be well done, but also its operating points must be determined. For an arbitrary digital circuit, its worst case delay determines the maximum speed (frequency) at which the circuit will operate as expected. Therefore, Static-Timing Analysis provides a key measurement for the circuit performace, which may as well be used for optimization purposes. This approach is considered supperior to testing the design with input vectors. Sometimes it is just impossible to enumerate all cases and arrive at the pattern that produces the worst case delay. Furthermore it is conservative, which means that it actually overestimates the true worst case delay of the circuit. This, unlike an approximate guess, guarantees the safe operation of the circuit.

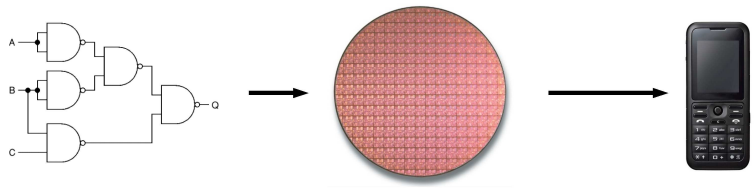
Static-Timing Analysis is a determenistic way of computing the delay imposed by the circuits design and layout. It is based on a predetermined set of possible events of process variations, also called corners of the circuit. The analysis is run for each of these corner-files and the worst case is then selected.

1.2 From Deterministic STA to Statistical STA

Although an excellent tool, current trends in process scalling have imposed significant difficulties to STA. As devices become smaller within-die variations' impact on circuit delay becomes more pronounced. Their impact on circuit delay is no longer insignificant, and unfortunately traditional STA has no rigorous method to handle them. Hence, deterministic analysis is no longer conservative and may result in either overestimation or underestimation of the circuit delay. Furthermore, as processes move deeper in the nanoscale range, the number of variations increases, which affects the running time of Deterministic STA (DSTA). Therefore, the need for another tool, which can resolve the aforementioned problems emerges and gives rise to Statistical STA (SSTA).

2 Statistical Static-Timing Analysis

2.1 Sources of Timing Variation



(a) *(b)* *(c)*

Figure 1: Sources of Uncertainty

There are three sources of timing variation that need to be considered, namely *Model Uncertainty*, *Process Uncertainty*, and *Environment Uncertainty*. Figure 1 illustrates the places of these variations. All three of these have, although unequal, contribution to the maximum delay of a an IC.

Model Uncertainty (*Figure 1a*). This uncertainty arises due to the imperfections in the models used during the design phase as well as inaccuracy in modeling the interconnect parasitics and inexactness in timing-analysis algorithms.

Process Uncertainty(*Figure 1b*). This is the uncertainty in the parameters of fabricated devices and interconnects (both die-to-die and within-die). These usually result due to lenses imperfections, mask perturbations and variations of the laser intensity.

Environment Uncertainty(*Figure 1c*). This includes the variations the fabricated device is exposed to once it is put in use. Such uncertainties are the operating voltage used and the temperature at which the device works.

Fortunately the first and the last sources of uncertainty may be treated with worst case scenarios and no further analysis is required. Therefore, only the Process Uncertainty needs deeper analysis and significantly more involvment as the worst case cannot be determined rightaway.

2.1.1 Sources of Process Variation (Process Uncertainty)

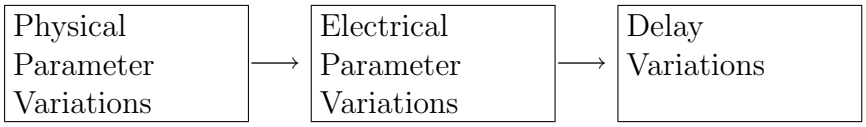


Figure 2: Variation Propagation

In order to understand how exactly process variations cause variations in the delay of an IC, their impact must be carefully traced. Starting with the uncertainty in the process, the

variations propagate onto the actual parameters of the devices manufactured. Therefore, at the end of the production there might be devices with different critical dimensions, oxide thickness, and channel doping. The width and thickness of the wires connecting them may also vary. The parameter variations on the other hand cause variations in the electrical characteristics of the circuit such as saturation current, gate capacitance, treshold voltage, wire capacitance and wire resistance. Finally, the electrical characteristics are the actual variables that determine the delay of a circuit. Thus, process variations ultimately result in delay variations. *Figure 2* illustrates the dependency.

Furthermore, there is one significant drawback of these variations. They might be in many cases correlated, as two or more parameter variations may occur due to a single process variation or multiple electrical parameters might share parameter dependency. One such example is the wire width which simultaneously affects the wire resistance and capacitance. With increase of the width the resistance decreases, but the parasitic capacitance grows and vice versa. This means that these two electrical characteristics are negatively correlated and ignoring this correlation might result in wrong timing analysis.

Now let us take a look at the variety of process variations (*Figure 3*). These can be basically split in two classes: *Systematic* and *Non-systematic*.

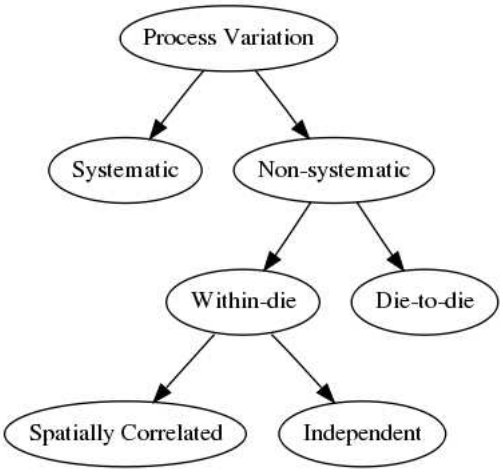


Figure 3: Types of Variation

The Systematic ones are these variations that are predictable upfront by analysing the layout. Therefore, they can be treated deterministically. Sometimes it is advantageous to model them in a probabilistic fashion and use this result early in the design phase before the actual layout is produced.

The Non-systematic variations are the truly random and uncertain component. They result from processes orthogonal to the design phase and, thus, are not affected by changes in the design. The only information available about them is their statistics. Therefore, they are modelled as random variables (*RVs*).

The latter case can be further split into subcategories as well. These include die-to-die

variations, which affect all devices on the same die in the same manner. However, different dies with the same chip layout may have different device parameters. These primarily result from lot to lot, wafer to wafer, reticle to reticle, and within reticle shifts. Another group is the within-die variations. These variations do not affect all devices within the same die equally. They, rather, gradually vary accross the area of the die and result with a circuit containing devices with different physical parameters. They are only caused by a within reticle variation in the confines of a single chip layout. These variations can be further divided into Spatially correlated and Independent ones. The first case affects closely spaced devices in a similar fashion and change gradually with position. The rest represent the residual variation which is independent for all devices on the chip. This type of variation is increasing in importance with process scalling.

2.2 Impact of Variation on Circuit Delay

Once the parameter variations and their respective distributions are known the challenge of computing the delay of the circuit emerges. For any circuit there are basically two types of delay that need to be computed. One is the total delay of a path consisting of devices connected in series (Single Path Delay). The second one is the maximum delay between two or more parallel paths (Maximum Delay of Multiple Paths).

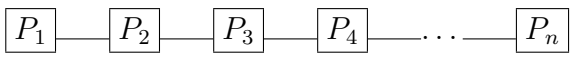


Figure 4: Devices connected in series

The most straightforward case is Single Path Delay with devices having independent delays. *Figure 4* depicts this case, where P_i refers to the delay probability of device i. Furthermore, let us assume that these probability densities are equal and normal distributed with mean μ and variance σ^2. Now the computation of the total delay of such a path becomes easy. The delay must be equal to the sum of all delays on the path. However, the sum of independent normal distributions results in a normal distribution with mean equal to the sum of the individual means and variance equal to the sum of the individual variances.

$$\sum_{i=1}^{n} \mathcal{N}(\mu, \sigma^2) = \mathcal{N}\left(\sum_{i=1}^{n} \mu, \sum_{i=1}^{n} \sigma^2\right) = \mathcal{N}(n\mu, n\sigma^2) \tag{1}$$

As a result the total coefficient of variation given by the ratio of deviation to mean

becomes smaller than the coefficient of variation of a single device on the path.

$$\left(\frac{\sigma}{\mu}\right)_{path} = \frac{\sqrt{n\sigma^2}}{n\mu} = \frac{1}{\sqrt{n}}\left(\frac{\sigma}{\mu}\right)_{gate} \tag{2}$$

Assuming independency definitely eases the computational effort, but in many cases this assumption is simply wrong. Therefore, this time the example path from *Figure 4* will have devices with again equal normal distributions (mean μ, variance σ^2), but this time the delay probabilities will be correlated with correlation coefficient ρ. Now the task of computing the total delay becomes a little bit more complicated. The mean of the total delay equals the sum of the means of the individual delays on the path. The variance, however, changes drastically. In addition to the sum of the individual variances on the path, a term describing the correlation between each two individual distributions is added.

$$\mu_{path} = n\mu \tag{3}$$

$$\sigma^2_{path} = \sum_{i=1}^{n}\sigma^2 + 2\rho\sum_{i=1}^{n}\sum_{j>i}^{n}\sigma_i\sigma_j = n\sigma^2(1+\rho(n-1)) \tag{4}$$

The above results give rise to the following expression describing the coefficient of variation. It now depends on the correlation coefficient.

$$\left(\frac{\sigma}{\mu}\right)_{path} = \frac{\sqrt{n\sigma^2(1+\rho(n-1))}}{n\mu} = \sqrt{\frac{1+\rho(n-1)}{n}}\left(\frac{\sigma}{\mu}\right)_{gate} \tag{5}$$

By close observation of *equation 5* it can be seen that a simple substitution of $\rho = 0$ (uncorrelatedness which implies independency) results in *equation 2*. Furthermore, if $\rho = 1$ (fully correlated delays) then the total coefficient of variation equals the coefficient of variation for a single device which is larger than the total one in the independent case. However, the mean is independent of the coefficient ρ and is the same in all cases. This means that the denominator in the fraction describing the total coefficient of variation is constant. Hence, it is the numerator (the standard deviation) that varies with the correlation. Therefore, for both independent and fully correlated case the resulting density function is around the same mean, only its spread changes. Given that the spread in the correlated case is larger, it can be concluded that this assumption results in overestimation of the total delay.

Another situation where the worst case delay needs to be determined is the case where multiple paths converge. Here, a probability density function of the maximum needs to be computed. In the following two paths with equal and normal total delay probability densities are considered.

Figure 5 shows the resulting density function of the maximum delay, given that the two paths are independent. It can be seen that the mean of the maximum is larger than

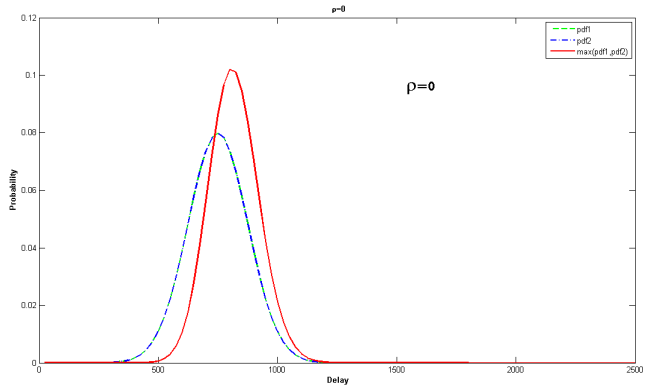


Figure 5: Independent ($\rho = 0$)

any of the original means and the shape closely, but not perfectly resembles a Gaussian density. The increase in the mean is caused by the fact that in three out of four cases the maximum delay is on the right side of the mean of the single path and only in one case on the left.

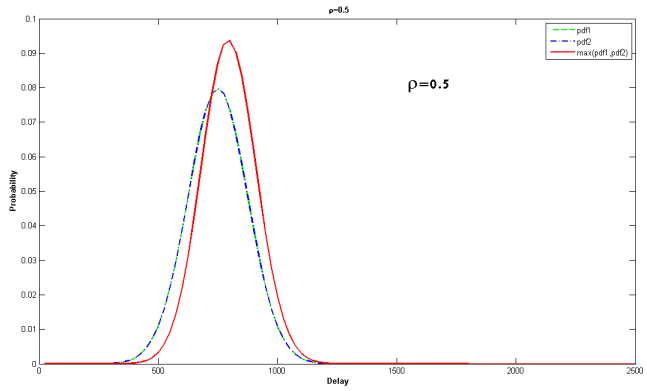


Figure 6: Correlated ($\rho = 0.5$)

As the correlation between the two paths increases, the resulting maximum density shifts to the left and its mean converges more to the mean of the two paths. *Figure 6* shows that for $\rho = 0.5$.

For perfectly correlated delay of the individual paths the result becomes trivial. Having two random variables with equal distributions, which are perfectly correlated, basically means observing one and the same random variable twice at a single instant of time. Thus, the distribution of the maximum will be equal to either one of the two single path delay distributions (*Figure 7*).

Because of the above results it can be concluded that the independent assumption will

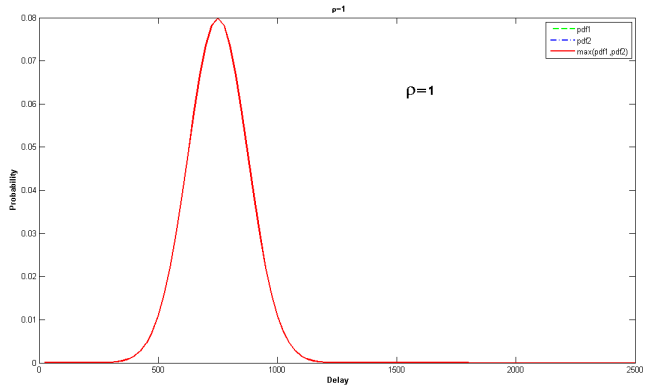


Figure 7: Correlated ($\rho = 1$)

overestimate the delay after a maximum operation and the correlated assumption will yield smaller result. The converse is true about the delay for a single path. Therefore, assumptions may be based on circuit topology. For a shallow circuit the maximum operation will dominate the worst case delay, hence the independent assumption might be used. For a significantly deeper circuit the delay of a single path will be dominant and, thus, the correlated assumption is expected to work.

2.3 Problem Formulation

Having introduced the basic notion of SSTA and its fundamental issues, now it is a good point to define and structure the problem that is faced by this approach.

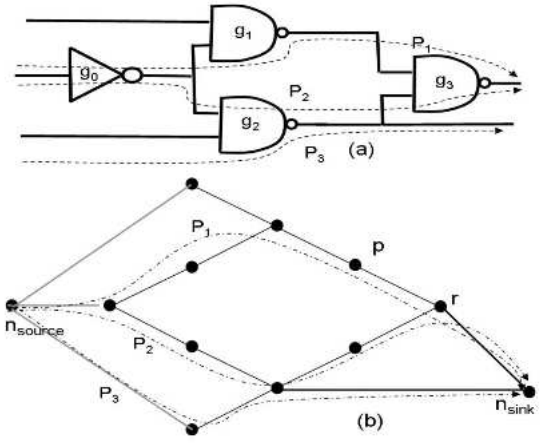


Figure 8: Combinatorial circuit and its corresponding DAG[1]

A Directed Acyclic Graph (DAG) G is constructed so that $G = \{N, E, n_s, n_f\}$. Where, N is the set of nodes corresponding to the input/output pins of the devices in the circuit, E is the set of edges connecting these nodes, each with weight d_i, and n_s, n_f are respectively source and sink of the graph. *Figure 8* shows a digital circuit and its corresponding DAG. This construction leads to the following definition.

Definition Let p_i be a path of ordered edges from source to sink in G. Let $D_i = \sum^k d_{i_j}$ be the path length of p_i. Then $D_{max} = max(D_1, \ldots, D_i, \ldots, D_n)$ is referred as the SSTA problem of the circuit.

In sequential circuits, just like in combinatorial ones, the delay of a path is computed as the sum of the individual edge delays. However, in this case the clock input acts as both source and sink. In the case of having a combinatorial logic bounded by two flip-flops, the analysis is performed by summing up all the times on the path between the two flip-flops plus the time for the clock signal to reach the first flip-flop. The delay between the clock source and the second flip-flop is then subtracted from this result. The reason for this is simple. In such a circuit it is desired that the propagation time of the new computation is much larger than the delay for passing the old result. Hence, the final delay has to be positive.

There are two main challenges in SSTA. The Topological Correlation which emerges from reconvergent paths, these are the ones which originate from a common node and then converge again at another node (reconvergent node). Such correlation complicates the maximum operation as it now has to be computed over correlated RVs. In *Figure 9* the two red paths reconverge at the rightmost gate.

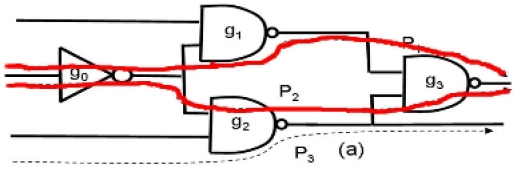


Figure 9: Toplogical Correlation

The second challenge is the Spatial Correlation. It arises due to device proximity on the die and gives raise to the problems of modeling delay and arrival time so that correlations are included, as well as preserving and propagating these correlations. *Figure 10* shows such two paths correlated by possibly placed closely gates.

There are many other challeges to SSTA. Nonnormal process parameters exist. Unlinke Gaussian distributions, these are not neccesserally rigourously handled by analytical approaches. Therefore, they impose great complications in calculating the delay. Furthermore electrical parameters also have nonlinear dependencies. As processes continue

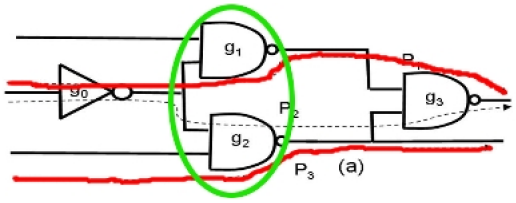


Figure 10: Spatial Correlation

to scale the linear approximation of these is no longer valid. Therefore, resulting delay distributions may not be normal at all.

Further considerations emerge because of the inheritently nonlinear maximum operation. Normal arrival times may result in a nonnormal delay after computing the maximum. The nonnormalities come from the skewness induced by this operation. Therefore, a method which can work with nonnormal distributions is highly desired. The following three figures exemplify the importance of the skewness in different cases.

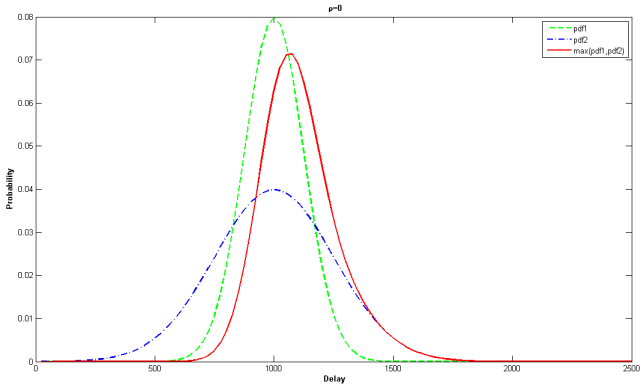


Figure 11: Two arrival times with same mean and different variances

In *Figure 11* the two paths over which the maximum is computed have same mean and different variances. The result of the computation is a positively skewed Gaussian density. It can be observed that the blue distribution is responsible for the skew as it dominates the maximum for values right of the mean. The probabilities of the green distribution for high delays diminish, while the ones from the blue distribution still have significant values. Simply ignoring the skewness will result in high delay error.

Figure 12 shows the resulting maximum of two identically distributed paths. The result highly resembles a normal distribution. However, there is a slight positive skew which will also cause error if ignored.

As it can be seen in *Figure 13* for arrival times with significantly different means it is safe to assume that the density resulting after maximum operation will be equal to the

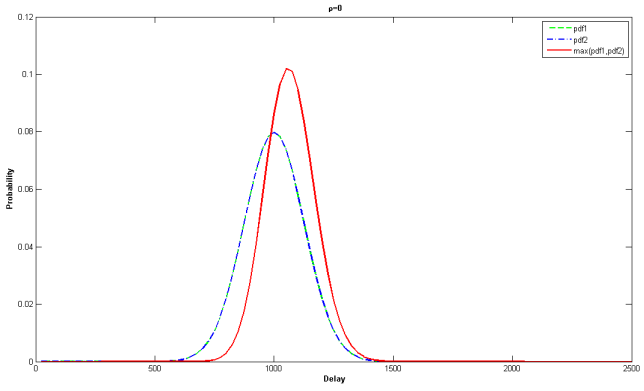


Figure 12: Two arrival times with same mean and same variance

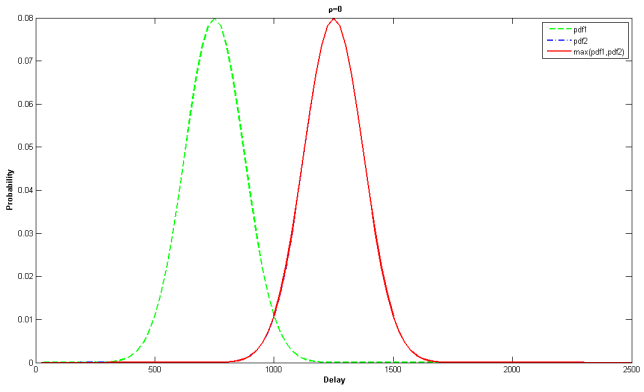


Figure 13: Two arrival times with different means and same variance

one of the arrival time with the higher mean. In the figure the blue density is completely covered by the red (maximum). Hence, in this case the result is normal.

2.4 Solution Approaches

The most general and brute froce method of solving the above mentioned problem is to use numerical integration. Although exact and applicable, this method is highly computationally expensive and, thus, undesired. This leads to another approach, namely, the use of Monte Carlo methods. The exact structure of these methods varies with the problem at hand. However, in general they all follow a common pattern: perform a statistical sampling of the sample space, perform deterministic computation for each sample, and aggregate the results into one final. In order to decrease the error, a lot of samples need to be taken,

which on the other hand increases the computation effort. Therefore, probabilistic analysis methods are highly desired. Two such exist, one is the *Path-based* approach and the other is the *Block-based* approach.

The Path-based approach constructs a set of likely to become critical paths. The delay for each of these paths is then computed and a statistical maximum is performed over these results to yield the worst case delay. However, there are several problems associated with this approach. Sometimes it is hard to construct a set of likely to become critical paths. Therefore, the worst case scenario can be unintentionally omitted. For highly balanced circuits the possibility of having to identify all paths as critical exists. This significantly increases the number of computations needed.

Therefore, it is desired to use the Block-based approach. There instead of constructing critical paths the whole graph is traversed node by node. For all fan-in edges to a node the associated delay is added to the arrival time at the source node (the node upstream of the current one). The final arrival time at the node is computed using a maximum operation over the previous results. This approach has the advantage of propagating only two times, the rise and the fall time.

2.4.1 Distribution Propagation Approaches

Analytical handling of distributions would be a good and computationally inexpensive approach. However due to the nonlinearities and nonnormalities that are to occur in the dependencies and distributions used, it becomes a task close to impossible. There exists ways of handling this problem analytically, but assumptions are inevitable part of them. Therefore, another way is to discretize the distributions and normalize them so that the discreet values sum up to 1. In this way new set of probability mass functions is constructed, which closely approximates the real densities.

Now summation is an easy task to do. The result of such an operation is just a sum of shifted and scaled values of the delay. The shifts and the magnitude of the scaling is determined by the distribution of the arrival time.

$$z = x + y \tag{6}$$

$$f_z(t) = f_x(1)f_y(t-1) + f_x(2)f_y(t-2) + \cdots + f_z(n)f_y(t-n) \tag{7}$$

$$f_z(t) = \sum_{i=-\infty}^{\infty} f_x(i)f_y(t-i) = f_x(t) * f_y(t) \tag{8}$$

Performing discrete time convolution is enough to compute the resulting delay from two devices in series.

In order to compute the maximum delay between two paths (x and y) two cases have to be considered. Either one of the path y has a particular delay and path x has a delay less than or equal to the one of x or vice versa (equation 10). In order to obtain a density

function this must be computed for all possible values of the delay t.

$$z = max(x, y) \tag{9}$$
$$f_z(t) = F_x(\tau < t) f_y(t) + F_y(\tau < t) f_x(t) \tag{10}$$

2.4.2 Handling Topological Correlations

Topological correlations emerge as paths reconverge. These correlations need to be carefully handled and propagated. One such way is constructing a Super-Gate. This device has a single fan-out and statistically independent inputs. The events at the input are then separately propagated, referred to as enumeration. Unfortunately for a Super-Gate with input vector of size n, the computational complexity in in the order of $O(c^n)$. Another way is to select and drop some of the topological correlations. This results in a total delay distribution $Q(t)$, which upper-bounds the original $P(t)$ for all t ($Q(t) \leq P(t), \forall t$)[2]. This results in a pessimistic analysis as the probability of having low delay is always smaller than the original one. Further inclusion of a lower-bounding distribution and the use of heuristics can approximate the original $P(t)$[3].

2.4.3 Correlation Models (Parameter Space)

In order to handle parameter correlations there exist a few sound models. The first one

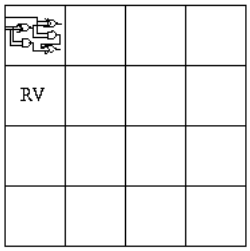


Figure 14: Grid Model

is the Grid model, where a the die area is divided by a square grid. Each square of the grid is assumed to correspond to a group of fully correlated devices. Therefore, each square is modeled as an RV, correlated with the RVs corresponding to the rest of the squares. The random variables are then whitened (a set of zero mean, unit variance normal random variables is constructed) and expressed as a linear combination of the new ones. In this way correlation is preserved by the means of sharing common dependencies.

Another one is called the Quadtree model[4]. It recursively divides the die area into four squares until individual gates fit into the grid. The partitions are stacked on top of each other. Each of the them is then assigned an independent RV. The random variable

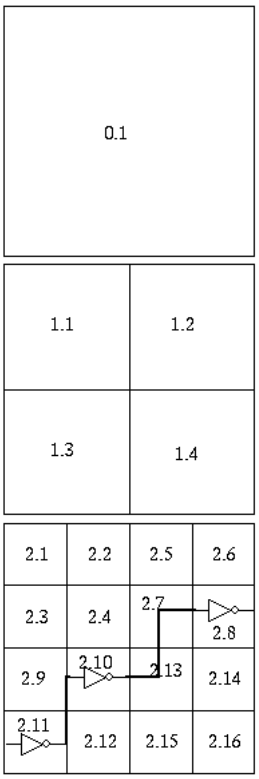


Figure 15: Quadtree Model

corresponding to the gate is computed by summing all areas that cover this particular device. Spatial correlation arises due to sharing common RVs on higher levels. In *Figure 15* gates at squares 2.11 and 2.10 have high correlation as they share RVs 1.3 and 0.1. However, gates 2.10 and 2.8 have lower correlation as they share only RV 0.1 . These results correspond to the expectation that closely spaced gates must have higher correlation than once spaced further apart.

Other models exist as well. Another way to handle the topological correlation is to assign four independent random variables to the four corners of the die [5]. The delay of each devices is then computed by the weighted sum of these four RVs. The weights are determined by the proximity of the device to each of the corners.

2.4.4 Propagation of Delay Dependence

Expressing the delay of each device by a linear combination of independent random variables leads to the creation of the cannonical form.

$$d_a = \mu_a + \sum_i^n a_i z_i + a_{n+1} R \tag{11}$$

Where μ_a is the nominal delay, a_i, $i \leq n$ are the coefficients (weights) in front of the independent RVs and the term $a_{n+1}R$ expresses the residual independent variation of the particular delay. It will be convenient to express both the sum and the maximum of such canonical forms in a canonical form. This will preserve the same approach throughout the computation of the delay for the whole circuit. Expressing the sum (C) of two canonical delays (A and B) is almost a straightforward task. The only unintuitive part is the coefficient of residual independent variation c_{n+1}. As the two coefficients, of which it is composed, correspond to independent (orthogonal) RVs, the new coefficient must be equal to the combined magnitude of the two.

$$C = A + B \tag{12}$$
$$\mu_c = \mu_a + \mu_b \tag{13}$$
$$c_i = a_i + b_i \quad \text{for} \quad 1 \leq i \leq n \tag{14}$$
$$c_{n+1} = \sqrt{a_{n+1}^2 + b_{n+1}^2} \tag{15}$$

Computation of the maximum is a significantly more involved. As the maximum operation is nonlinear, but the canonical form is, only an approximation of the maximum can be computed. The following is an algorithm proposed for solving this problem [6].

First of all the variance and covariance of the canonical forms A and B need to be calculated.

$$\sigma_a^2 = \sum_i^n a_i^2 \quad \sigma_b^2 = \sum_i^n b_i^2 \quad r = \sum_i^n a_i b_i \tag{16}$$

Then the probability of $A > B$ also called the tightness probability needs to be computed [7].

$$T_A = \Phi\left(\frac{\mu_a - \mu_b}{\theta}\right) \tag{17}$$
$$\Phi(x') = \int_{-\infty}^{x'} \phi(x) dx \tag{18}$$
$$\phi(x) = \frac{1}{\sqrt{2\pi}} \exp^{-\frac{x^2}{2}} \tag{19}$$
$$\theta = \sqrt{\sigma_a^2 + \sigma_b^2 - 2r} \tag{20}$$

The new mean and variance of the new canonical form $C = max(A, B)$ have to be expressed.

$$\mu_c = \mu_a T_A + \mu_b(1 - T_A) + \theta\phi\left(\frac{\mu_a - \mu_b}{\theta}\right) \tag{21}$$

$$\sigma_c^2 = (\mu_a + \sigma_a^2)T_A + (\mu_b + \sigma_b^2)(1 - T_A) + (\mu_a + \mu_b)\theta\phi\left(\frac{\mu_a - \mu_b}{\theta}\right) - \mu_c^2 \tag{22}$$

Then the weighting coefficients for the maximum.

$$c_i = a_i T_A + b_i(1 - T_A) \quad for \quad 1 \leq i \leq n \tag{23}$$

At last the coefficient of free variation c_{n+1} has to be determined. Its derivation comes from the fact that the estimate has to be consistent, i.e. the variaton must be equal to the true one. Therefore, if from the true variance σ_c^2 the sum of all variances c_i^2 is subtracted, the remainder will be equal to the variation coming from the residual term. In a similar fashion, the last coefficient can be computed.

Unfortunately, this approach only computes an estimate, which by no means guarantees conservative results. Therefore, it is not suitable as it might underestimate the delay on some occasions. Another way of coping with the problem is the use of the following relation.

$$max\left(\sum_i^n a_i, \sum_i^n b_i\right) \leq \sum_i^n max(a_i, b_i) \tag{24}$$

This result guarantees that if the higher of the coefficients correspoding to a particular independent RV is selected, then the result will be conservative. Therefore, a bouding canonical C_{bound} form of the delay can be constructed by selecting the higher mean and the largest coefficients.

$$\mu_c = max(\mu_a, \mu_b) \tag{25}$$

$$c_{bound_i} = max(a_i, b_i) \tag{26}$$

2.4.5 Nonlinear and Nonnormal Approaches

Because of the existance of nonnormal distributions and nonlinear dependencies, special canonical forms have been developed to cope with these challenges. All of these are handeled by numerical computations and tightness probabilities. In order to include the effect of nonlinear dependencies additional term is included in the form.

$$d_a = \mu_a + \sum_i^n a_i z_i + \sum_{i=1}^n \sum_{j=1}^n b_{ij} z_i z_j + a_{n+1} R \tag{27}$$

For the nonnormal distributions the same approach is used. The delay depends has terms for both the normally distributed contributions and the nonnormal ones.

$$d_a = \mu_a + \sum_i^n a_i z_i + \sum_j^m a_{n+j} z_{n+j} + a_{n+m+1} R \tag{28}$$

Equations 27 and 28 can be aggreated in the following common form.

$$d_a = \mu_a + \sum_i^n a_i z_i + f(z_{n+1}, \ldots, z_{n+m}) + a_{n+1} R \tag{29}$$

3 Conclusion

Statistical Static-Timing Analysis has gained excessive interest in recent years. It is a relatively newly developed approach and currently there are number of commercial efforts underway to utilize this approach and use it.

However, there are still many features of DSTA that are not addressed by SSTA. Hence, the determenistic approach still has significant advantage over the statistical one. Considerations that need to be included in SSTA are coupling noise, clock issues, as it SSTA can become really complicated for sequential logic, and complex delay modelling as well as others. Furthermore, SSTA must move beyond the point of serving as an analysis tool into the sphere of actual optimization of digital circuits.

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