Development and research of different architectures of I^2C bus controller

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I2C and its alternatives

I²C (**Inter-Integrated Circuit**) is a multi-master serial computer bus invented by Philips that is used to attach low-speed peripherals to a motherboard, embedded system, or cellphone

Name	Description	Advantages over I2C	Disadvantages over I2C
SPI	Synchronous serial connection, 3 or 1 line for transmission, data is sent synchronized by the clock, transmission is based on push/pull technology	Higher speed	No addressing (many devices on one bus are not allowed)
UART	Universal Asynchronous Receiver/Transmitter. Fixed baudrate is used for transmission.	Ability to serve as master and slave at the same time. Physical layer can be used, allowing to bridge larger distances	No addressing (many devices on one bus are not allowed)
CAN	Complex protocol of CAN allows for data integrity check, device addressing, error recovery and several advanced features	Physical layer can be used, allowing to bridge larger distances	Complexity
1-Wire®	Just one wire plus ground are used (i.e. two wires). It is even possible to supply power to connected components over these two wires.	Physical layer can be used, allowing to bridge larger distances	Strict time keeping on both, master and slave side, lower speed

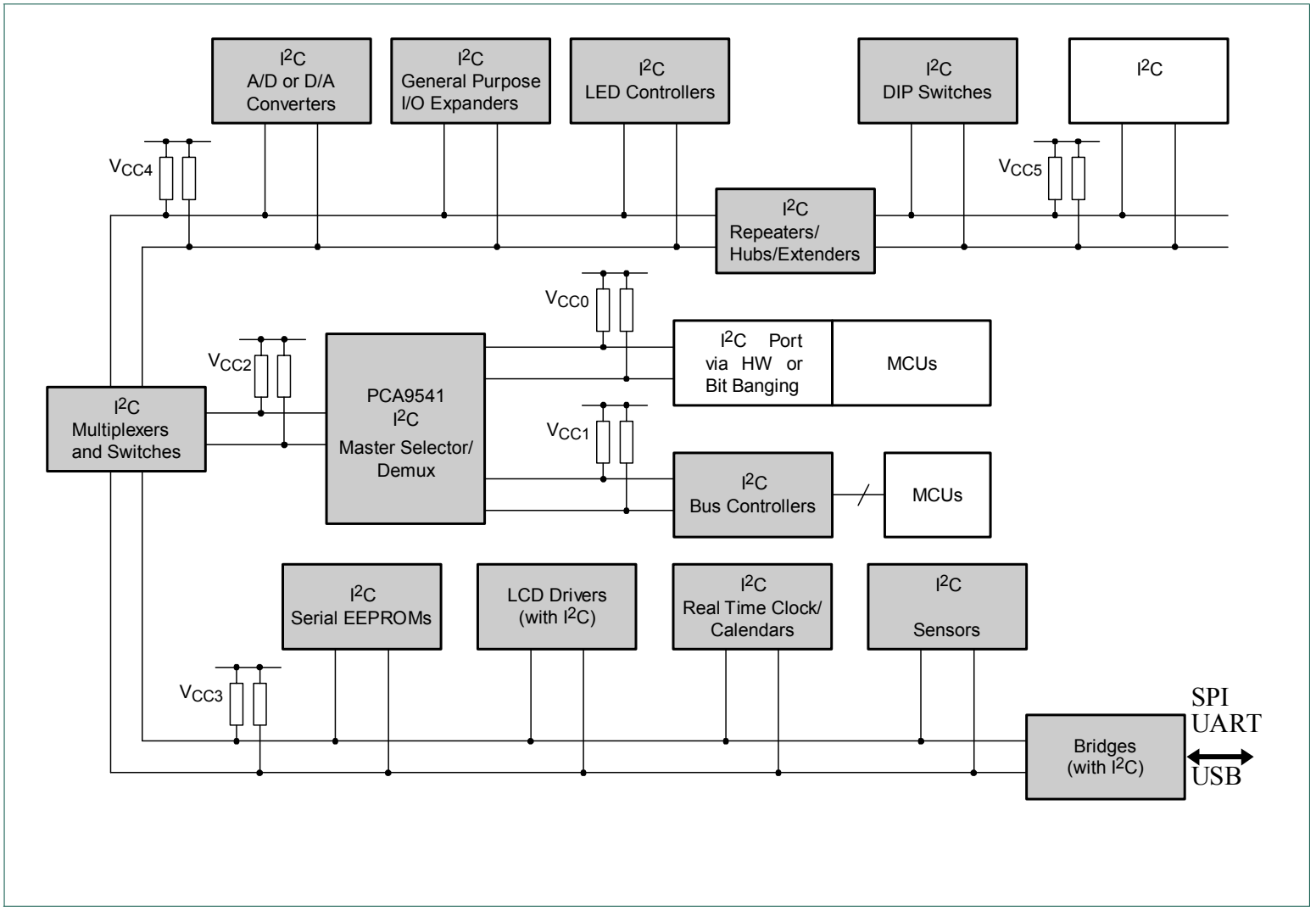
Designer benefits

- Functional blocks on the block diagram correspond with the actual ICs; designs proceed rapidly from block diagram to final schematic
- No need to design bus interfaces because the I2C-bus interface is already integrated on-chip
- Integrated addressing and data-transfer protocol allow systems to be completely software-defined
- The same IC types can often be used in many different applications
- Design-time reduces as designers quickly become familiar with the frequently used functional blocks represented by I2C-bus compatible IC
- ICs can be added to or removed from a system without affecting any other circuits on the bus
- Fault diagnosis and debugging are simple; malfunctions can be immediately traced
- Software development time can be reduced by assembling a library of reusable software modules

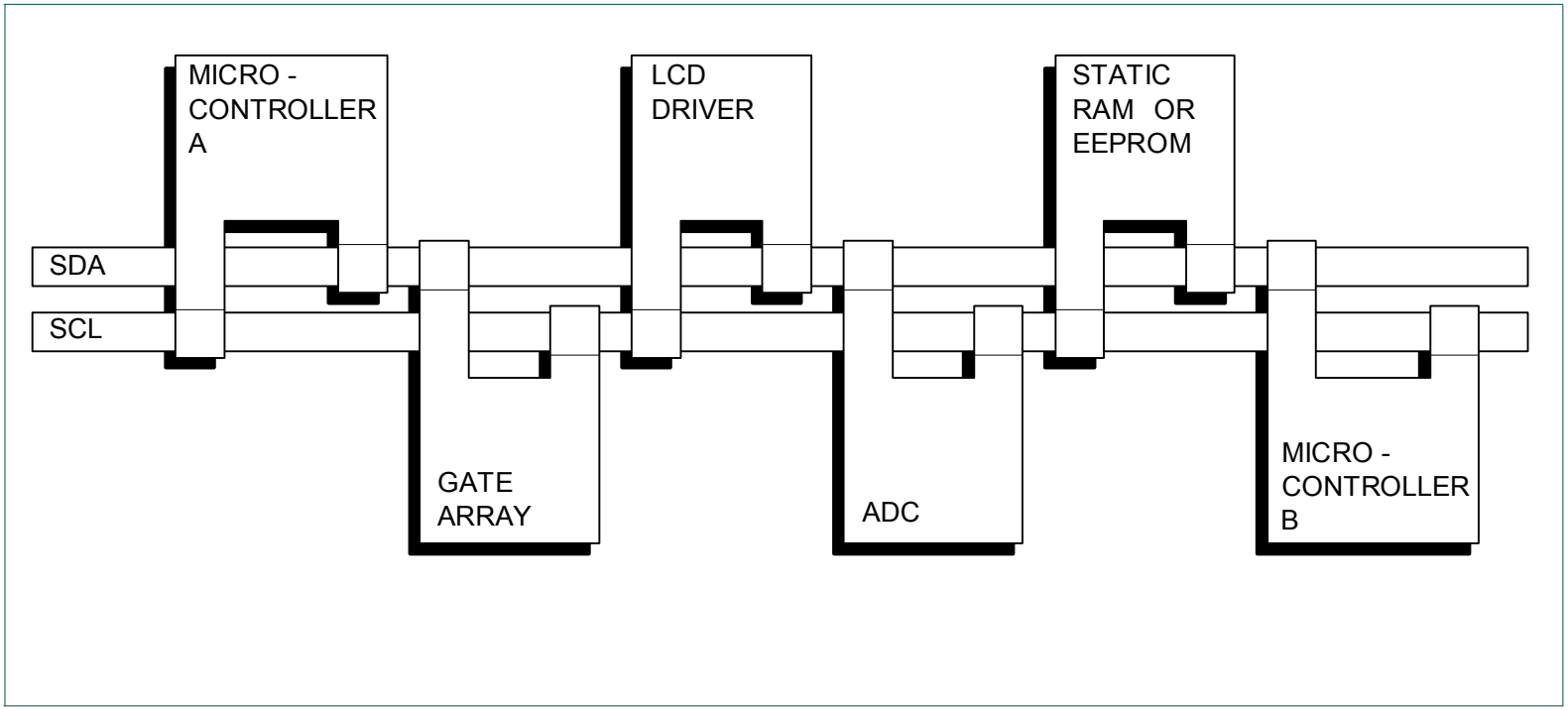
Manufacturer benefits

- The simple 2-wire serial I2C-bus minimizes interconnections so ICs have fewer pinsand there are not so many PCB tracks; result — smaller and less expensive PCBs
- The completely integrated I2C-bus protocol eliminates the need for address decoders and other ‘glue logic’
- The multi-master capability of the I2C-bus allows rapid testing and alignment of end-user equipment via external connections to an assembly-line

Example of I²C bus applications



Example of an I2C-bus configuration using two microcontrollers

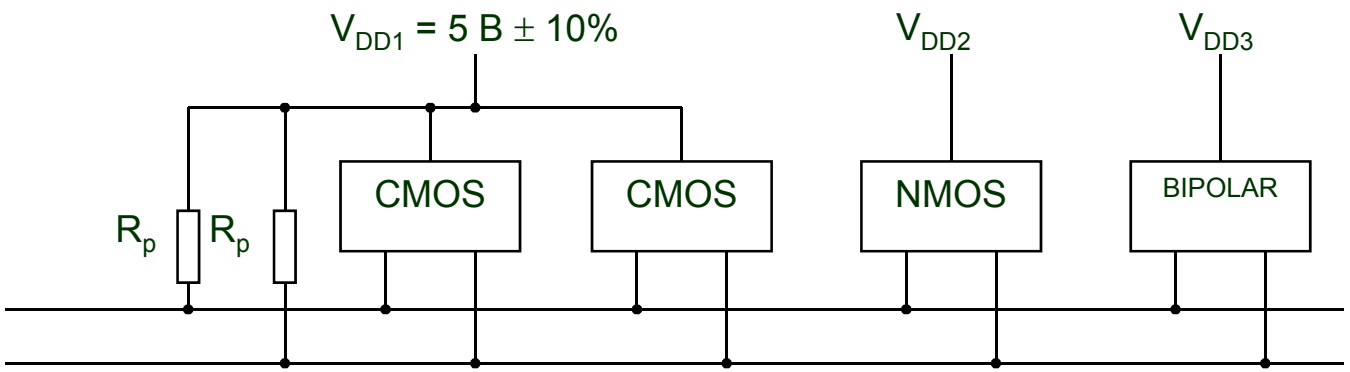


Applicability of I2C-bus protocol features

Feature	Configuration		
	Single master	Multi-master	Slave
START condition	M	M	M
STOP condition	M	M	M
Acknowledge	M	M	M
Synchronization	n/a	M	n/a
Arbitration	n/a	M	n/a
Clock stretching	O	O	O
7-bit slave address	M	M	M
10-bit slave address	O	O	O
General Call address	O	O	O
Software Reset	O	O	O
START byte	n/a	O	n/a
Device ID	n/a	n/a	O

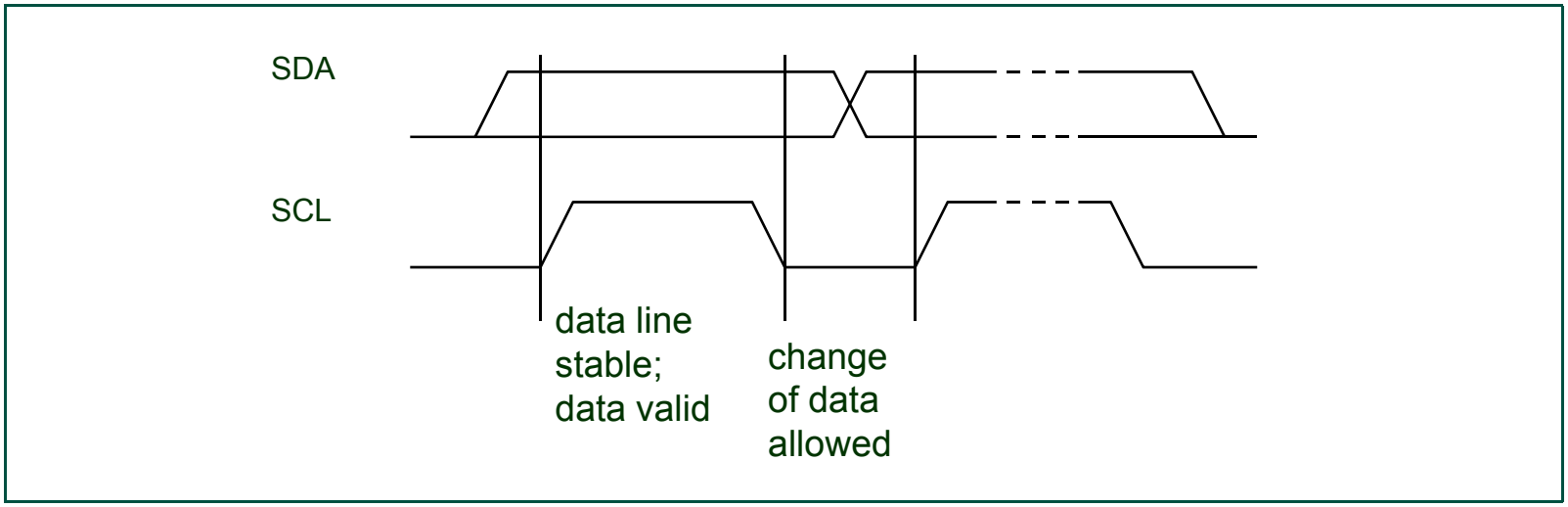
M = mandatory; O = optional; n/a = not applicable.

Devices with a variety of supply voltages sharing the same bus

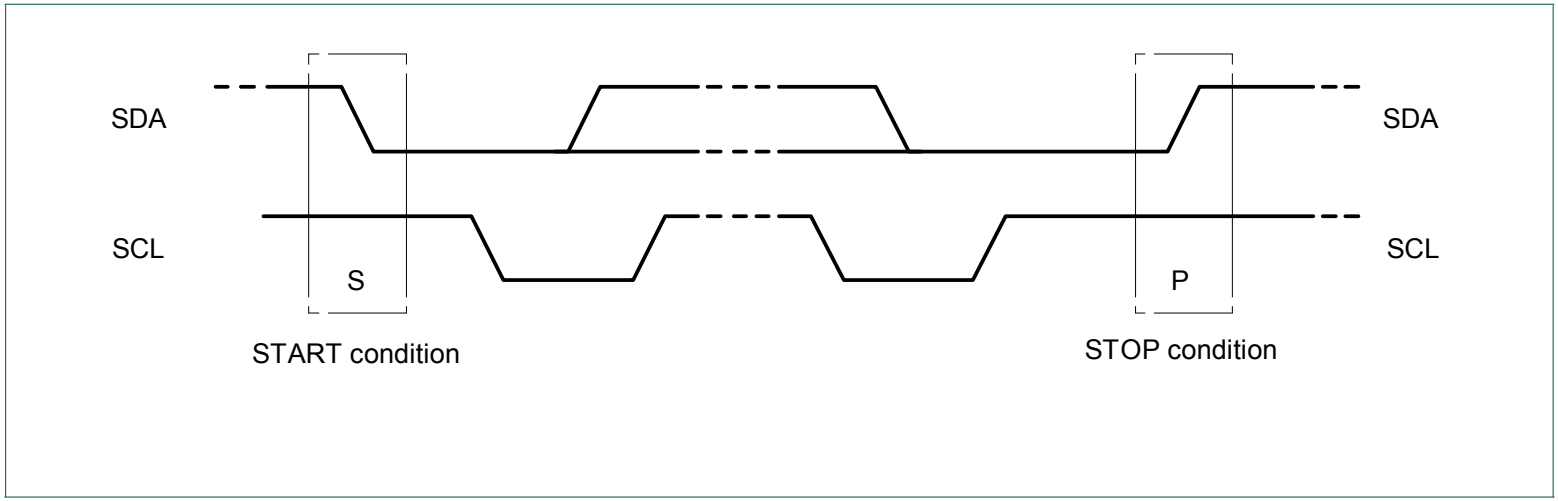


V_{DD2} and V_{DD3} are device dependent (e.g., 12 V).

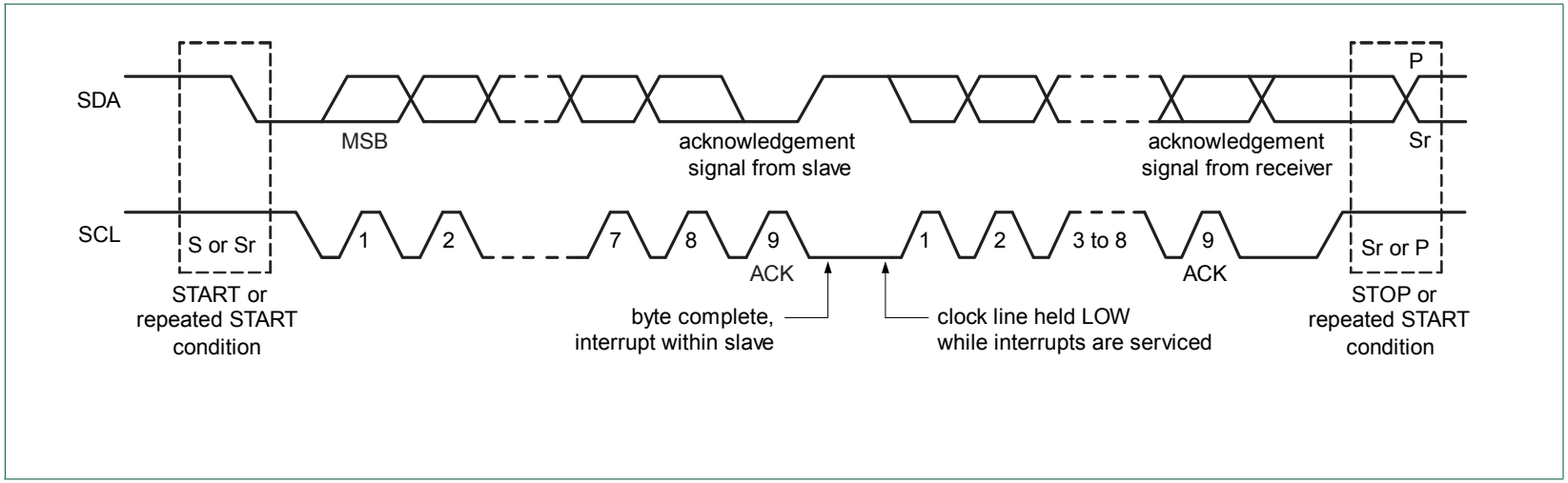
Bit transfer on the I2C-bus



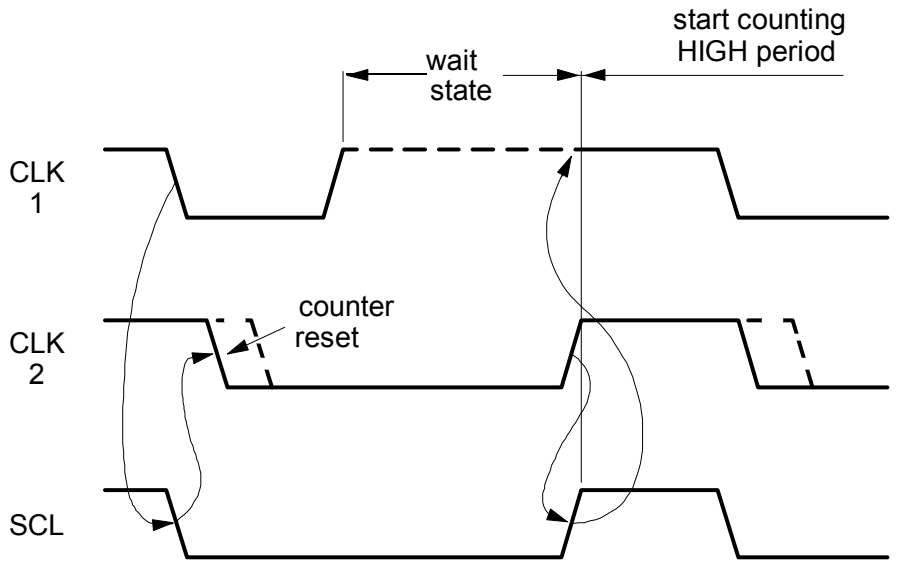
START and STOP conditions



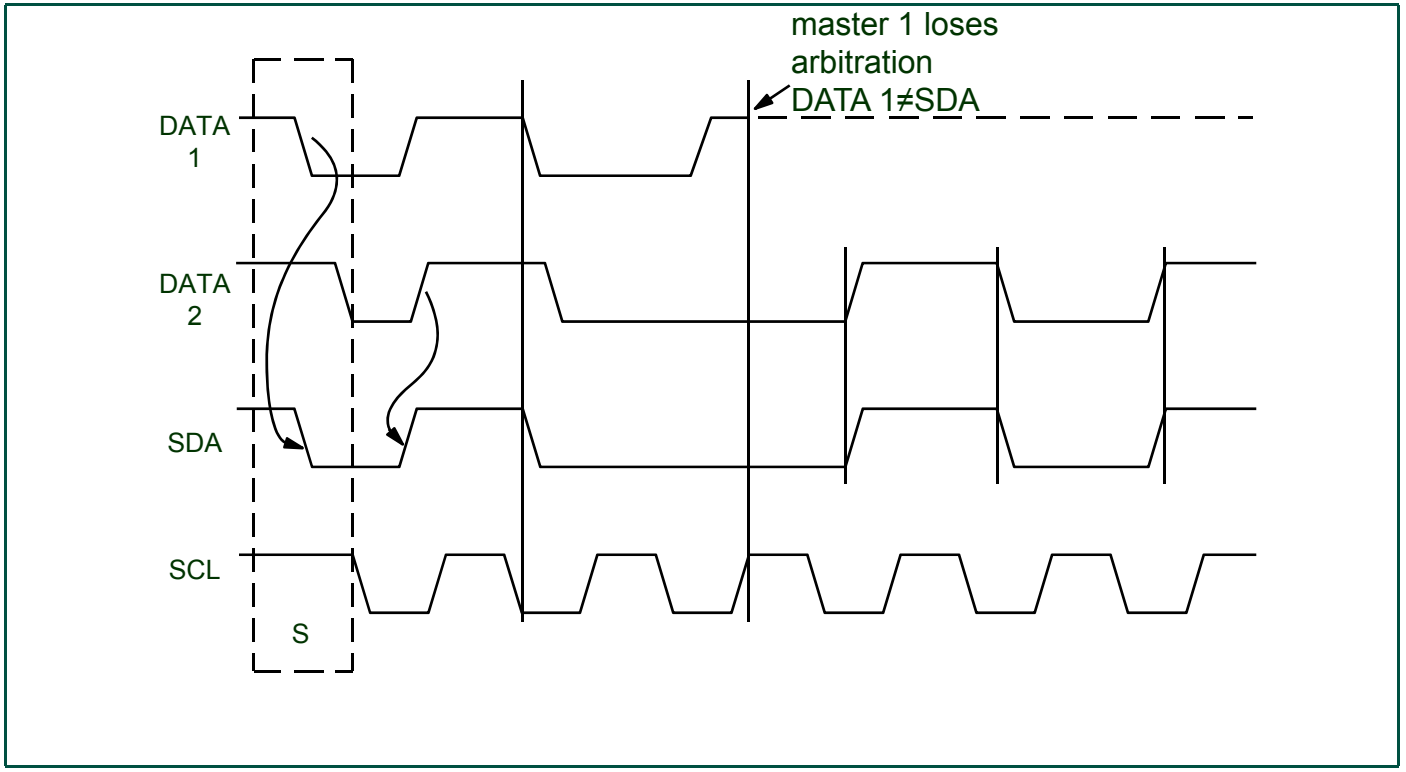
Data transfer on the I2C-bus



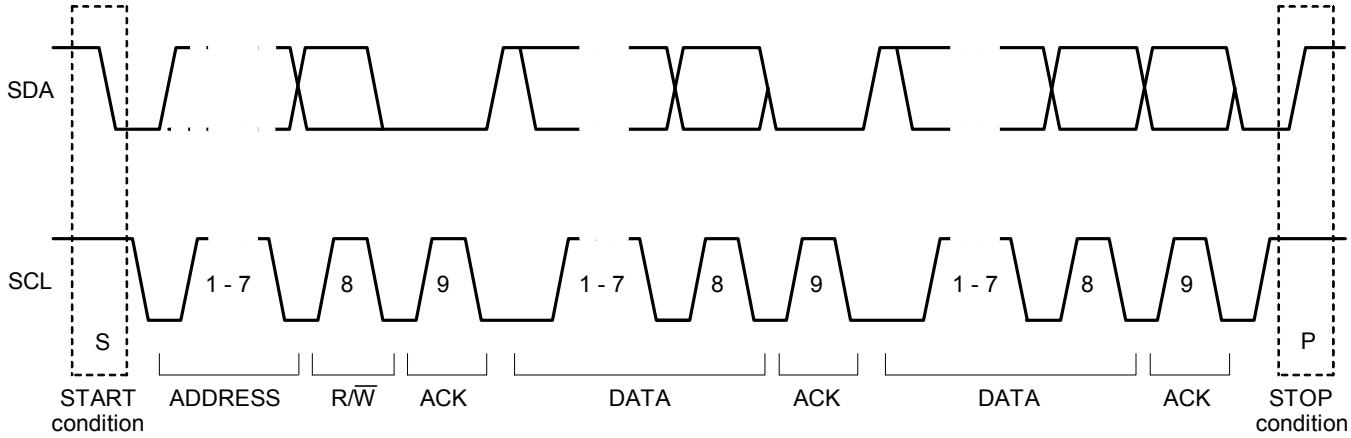
Clock synchronization during the arbitration procedure



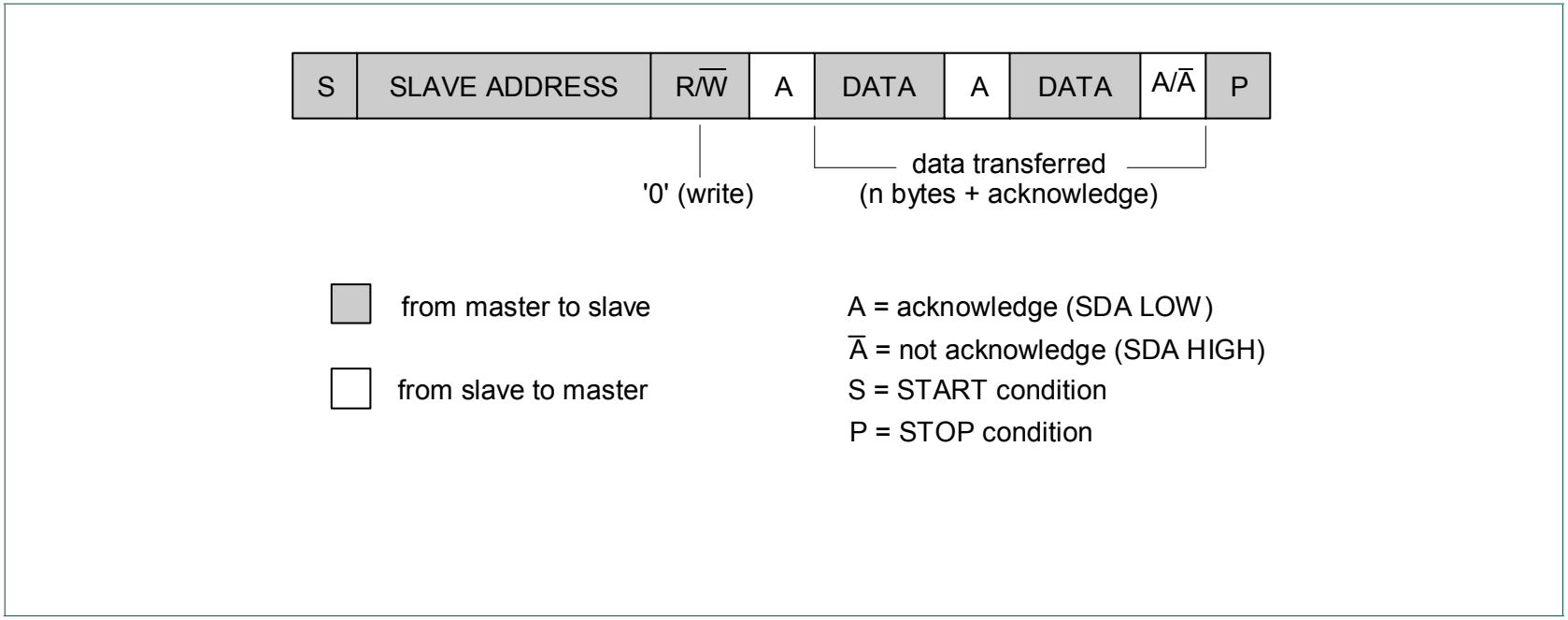
Arbitration procedure of two masters



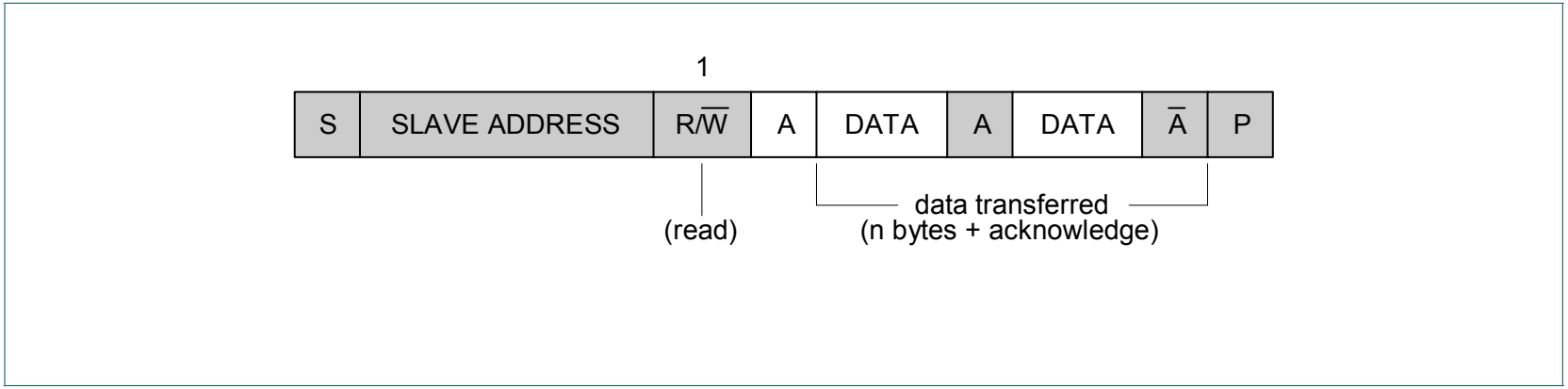
A complete data transfer



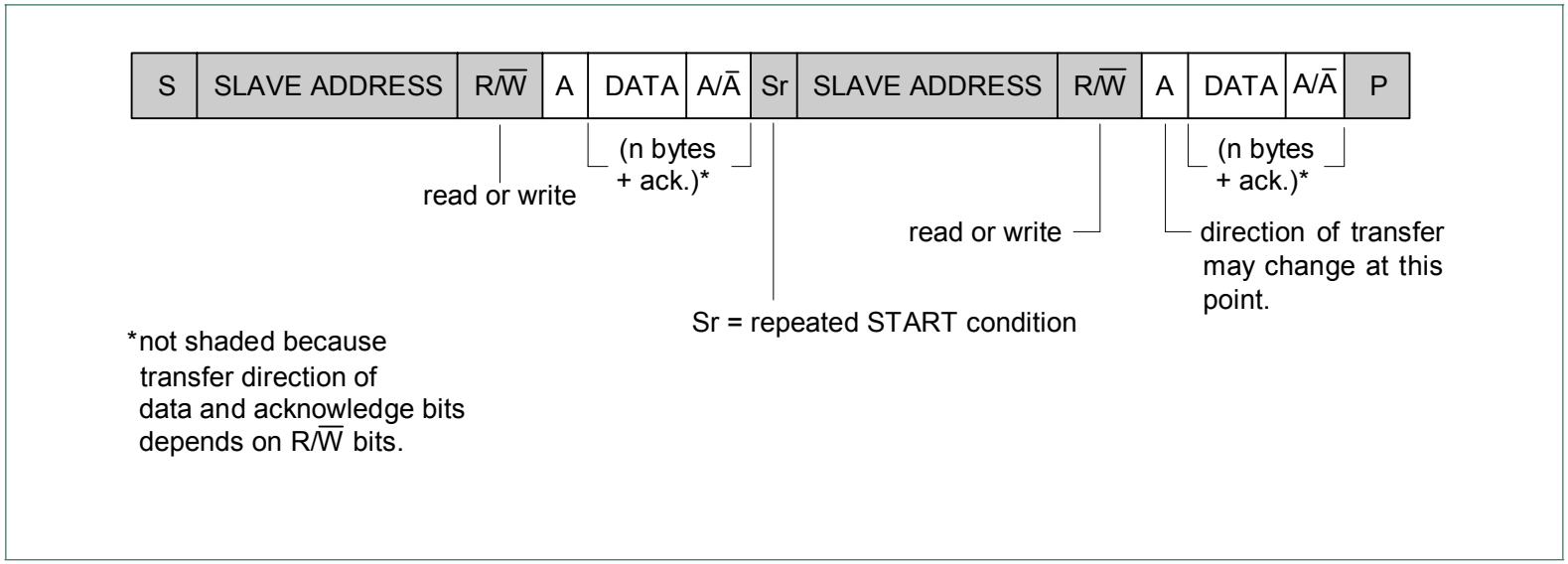
A master-transmitter addressing a slave receiver with a 7-bit address (the transfer direction is not changed)



A master reads a slave immediately after the first byte



Combined format



Bus speeds

- **Standard-mode (Sm)**, with a bit rate up to 100 kbit/s
- **Fast-mode (Fm)**, with a bit rate up to 400 kbit/s
- **Fast-mode Plus (Fm+)**, with a bit rate up to 1 Mbit/s
- **High-speed mode (Hs-mode)**, with a bit rate up to 3.4 Mbit/s.

I2C applications

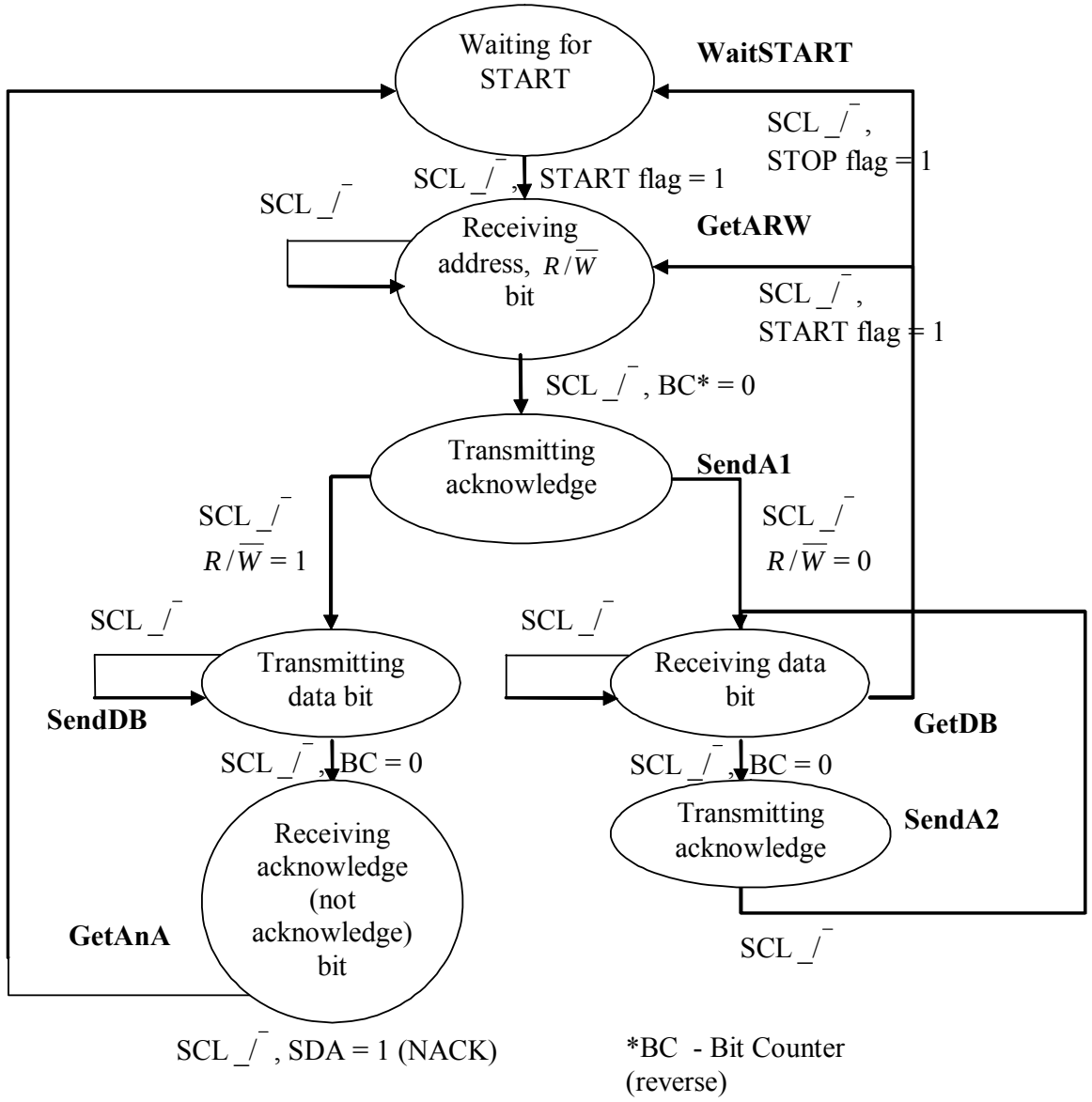
I²C is appropriate for peripherals where **simplicity** and **low manufacturing cost** are more important than **speed**. Common applications of the I²C bus are:

- Reading configuration data from SPD EEPROMs on SDRAM, DDR SDRAM, DDR2 SDRAM memory sticks (DIMM) and other stacked PC boards
- Supporting systems management for PCI cards, through an SMBus 2.0 connection.
- Accessing NVRAM chips that keep user settings.
- Accessing low speed DACs and ADCs.
- Changing contrast, hue, and color balance settings in monitors (Display Data Channel).
- Changing sound volume in intelligent speakers.
- Controlling OLED/LCD displays, like in a cellphone.
- Reading hardware monitors and diagnostic sensors, like a CPU thermostat and fan speed.
- Reading real time clocks.
- Turning on and turning off the power supply of system components.

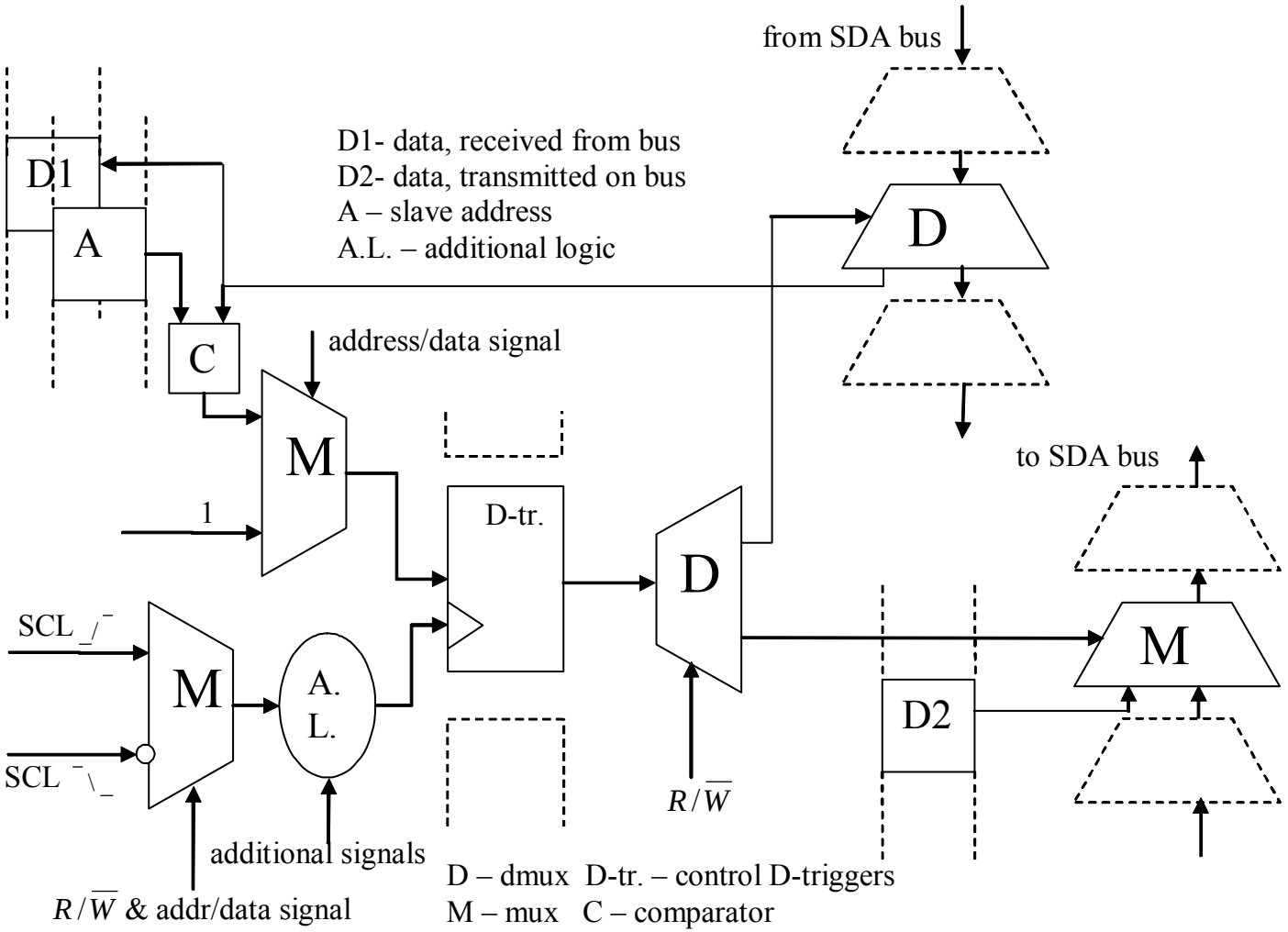
Architectures of I^2C bus controller

- State machine architecture
- Demultiplexer/Multiplexer chains architecture
- Two shift registers architecture

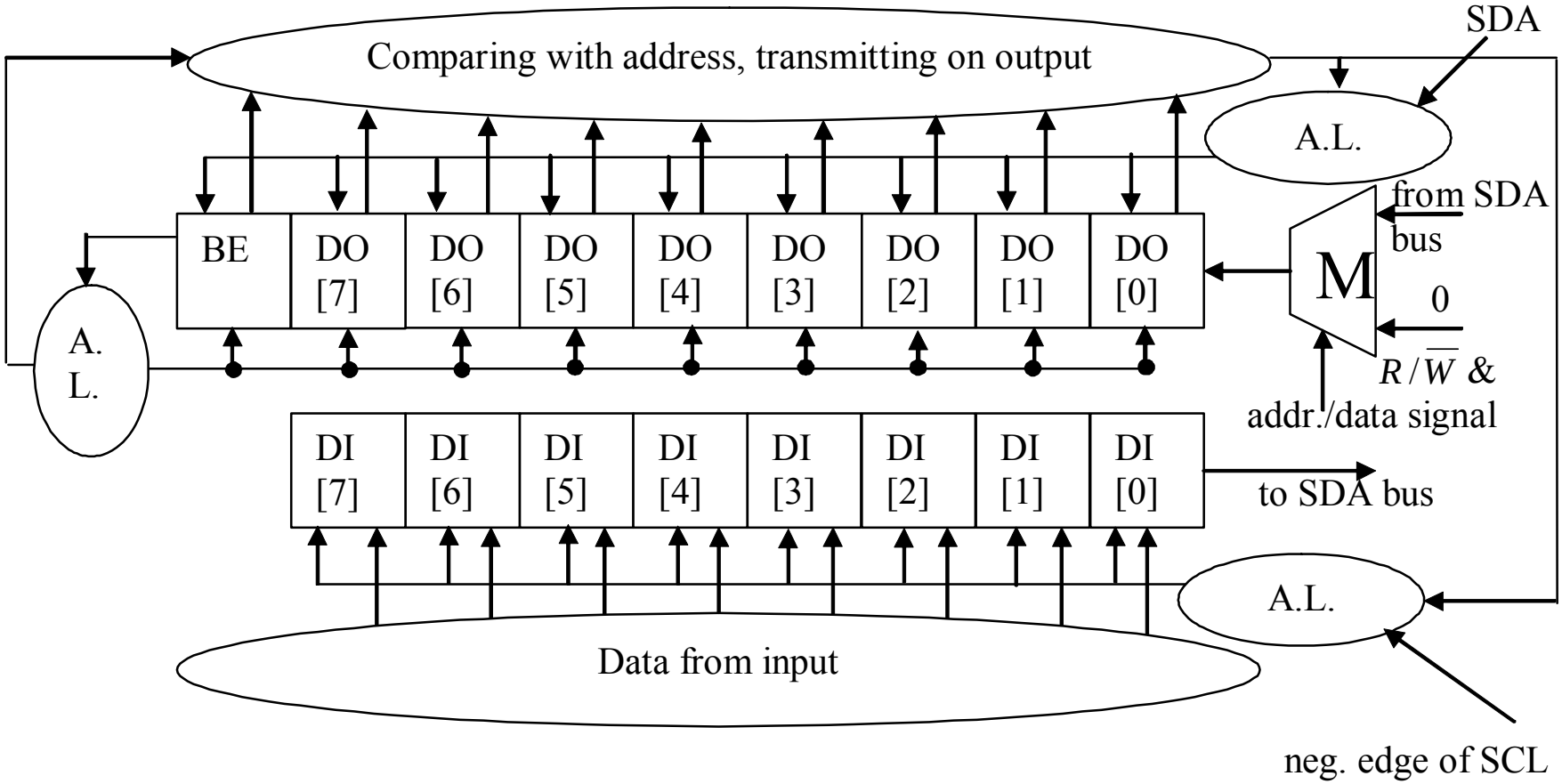
Mealy state machine for slave I²C bus contoller



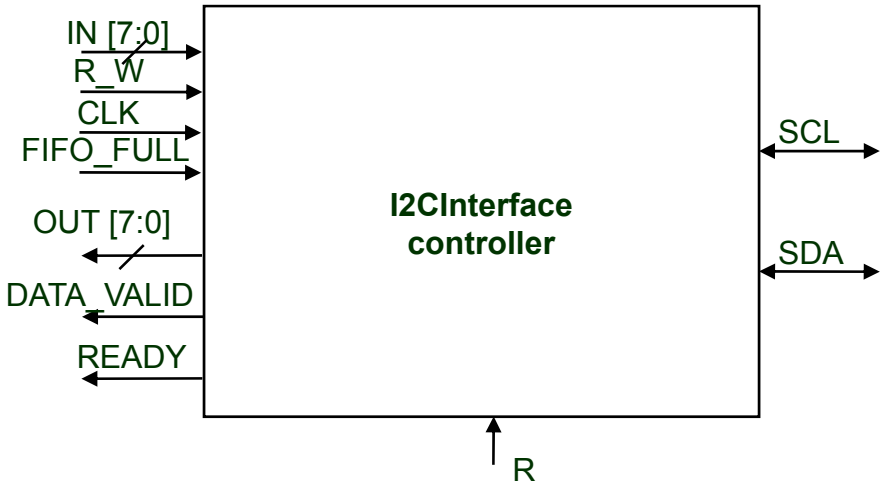
Demultiplexer/Multiplexer chains architecture of slave I2C bus controller



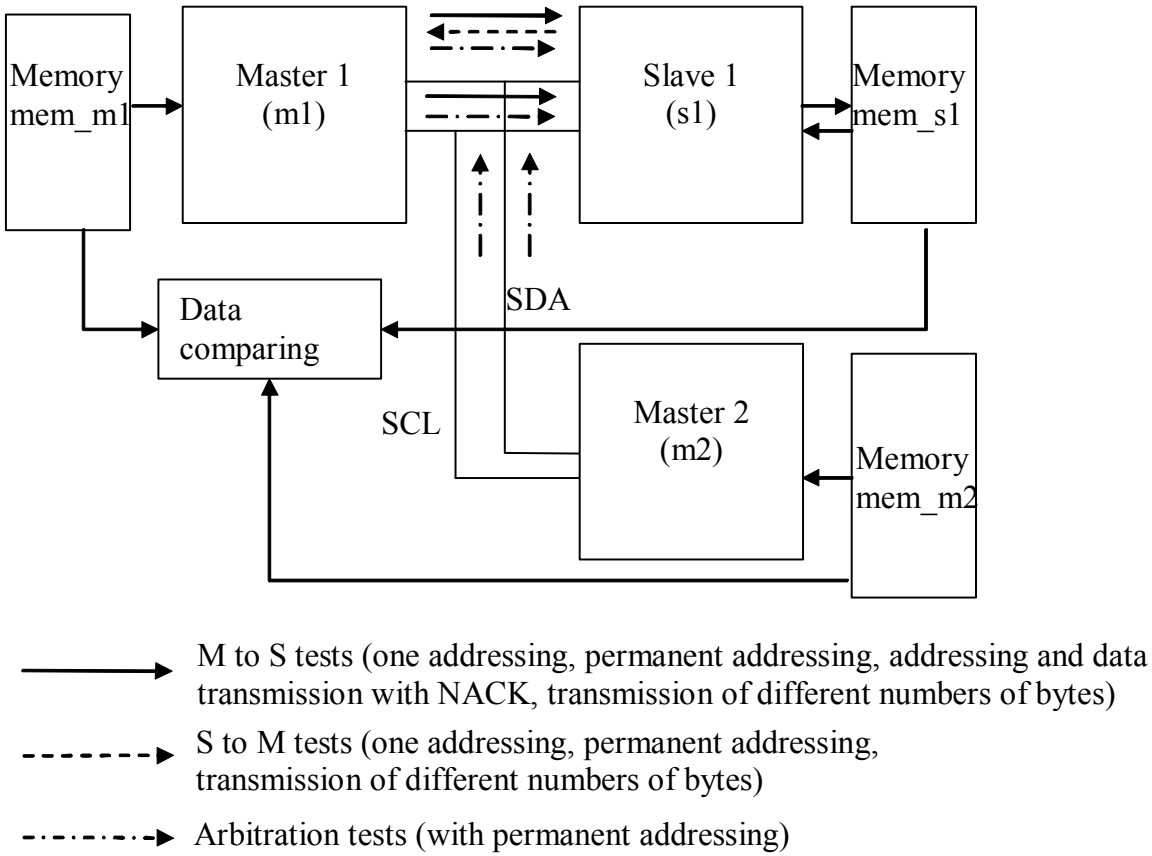
Two shift registers architecture of slave I²C bus controller



Symbol of slave I2C bus controller



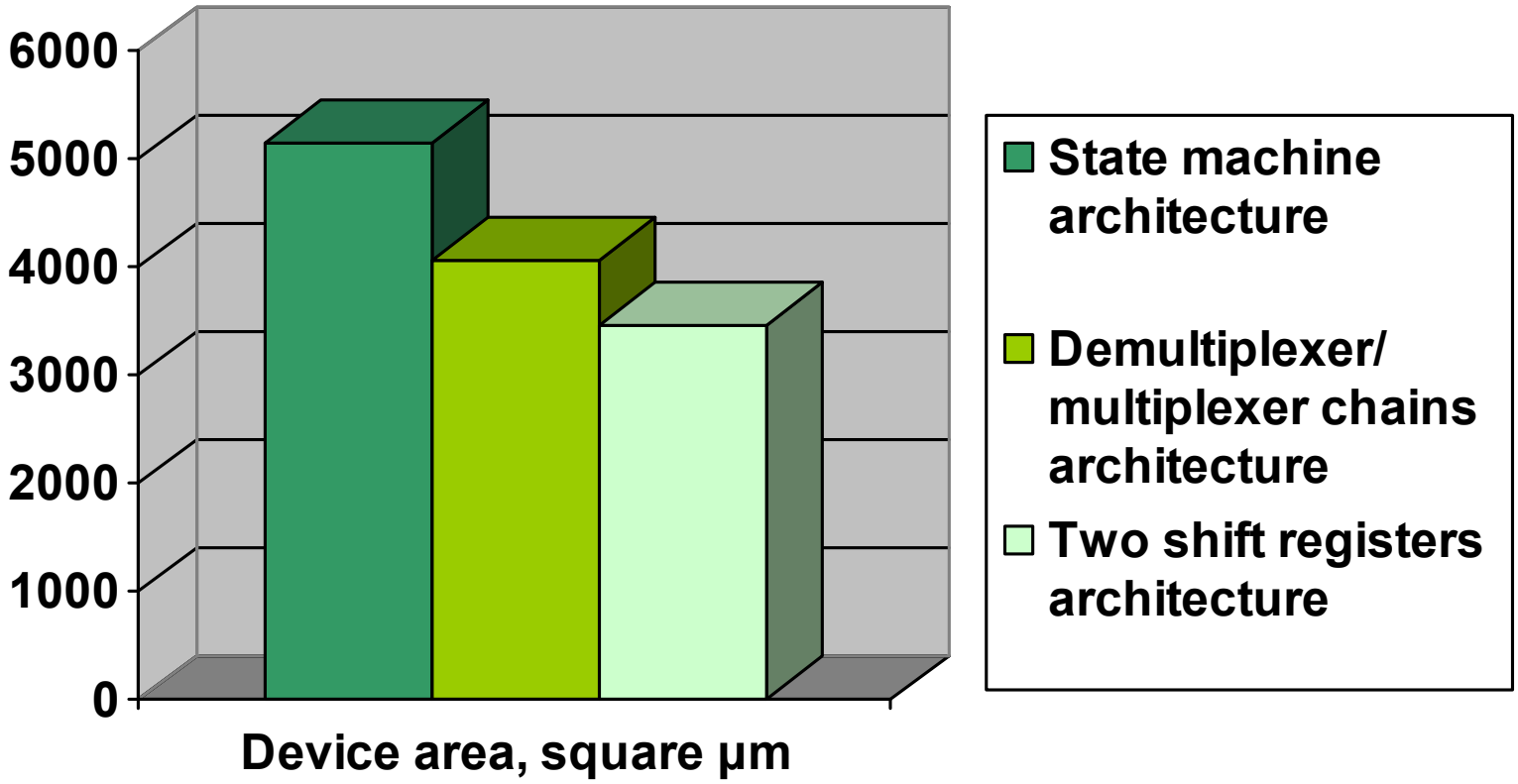
Verification of slave I2C bus controller



Comparative characteristics of I2C bus architectures

Architecture name	Area of non-combina-tional elements (triggers), µm	Area of combina-tional elements, µm	Number of cells	Whole-time addre-ssing	Number of nets
State machine architecture	2031,6	3108,9	194	No	216
Multiplexer/ demultiplexer chains architecture	2056,2	1990,7	144	No	168
Two shift registers architecture	2011,1	1445,9	102	Yes	127

Area of architectures (data are based on cell areas)



Power of architectures (data are based on cell powers)