Analysis of schematic approaches for reducing the static power consumption of VLSI and SoC functional blocks.

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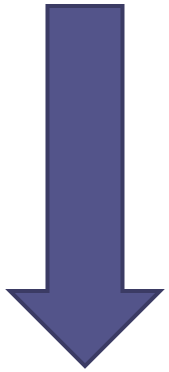
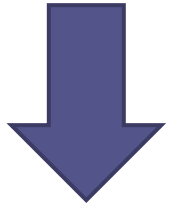
Background

Transistor size becomes smaller and smaller



Transistors become faster and faster



High density

V_{th} falls

Increase of leakage power

Leakage power sources

- Subthreshold leakage

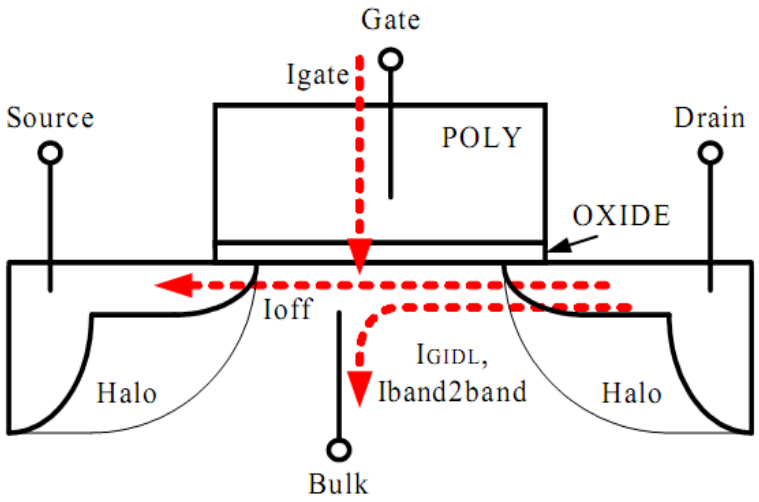
✓Leakage increases exponentially as V_T decreases

✓Short-channel effect: channel controlled by drain

$$I_{sub} = \frac{\mu W C_{ox}}{L} V_T^2 e^{\frac{|V_{GS}| - |V_t|}{\eta V_T}} \left(1 - e^{\frac{-|V_{DS}|}{V_T}}\right)$$

- Gate-oxide leakage

✓Gate tunneling due to thin oxide



Schematic approaches for reducing the static power: classification

State-destructive techniques

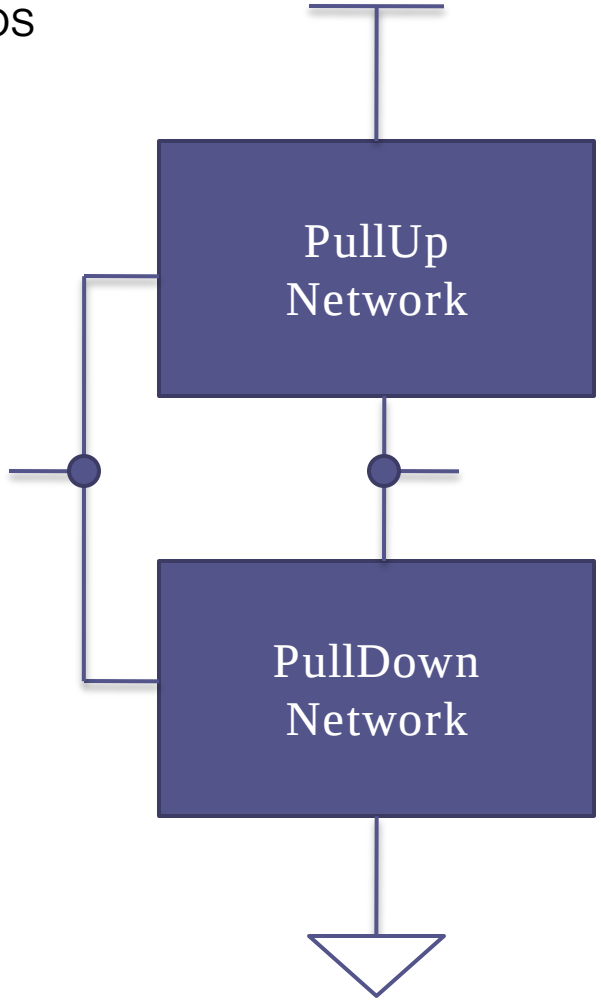
- ✓ Sleep approach
- ✓ Zig-zag approach

State-preserving techniques

- ✓ Stack approach
- ✓ Sleepy stack approach
- ✓ Feedback using inverter
- ✓ Sleepy keeper

Schematic approaches for reducing the static power

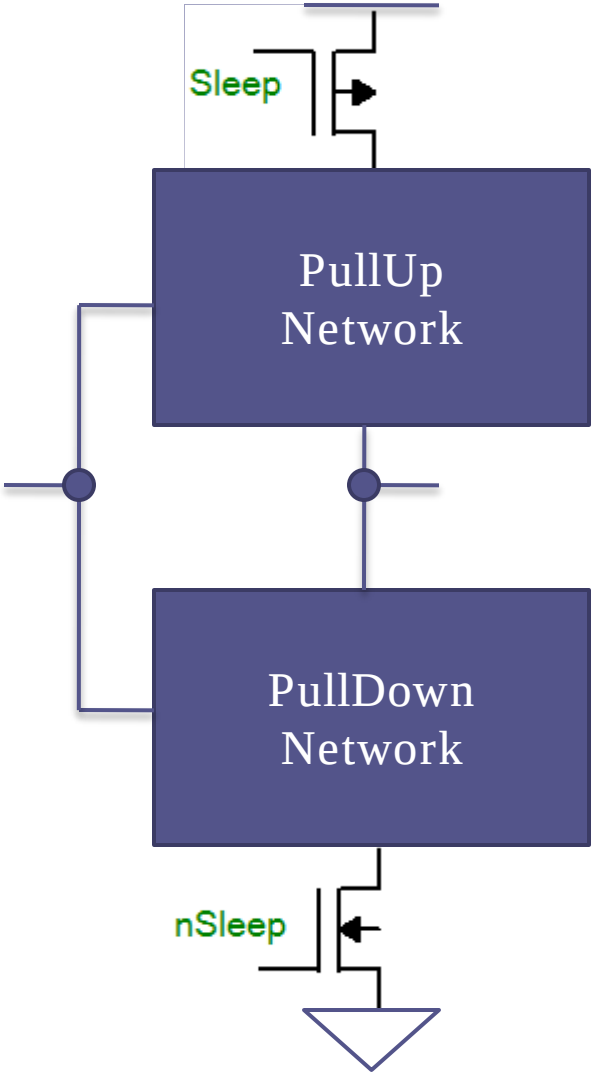
The base CMOS



Schematic approaches for reducing the static power

Sleep approach

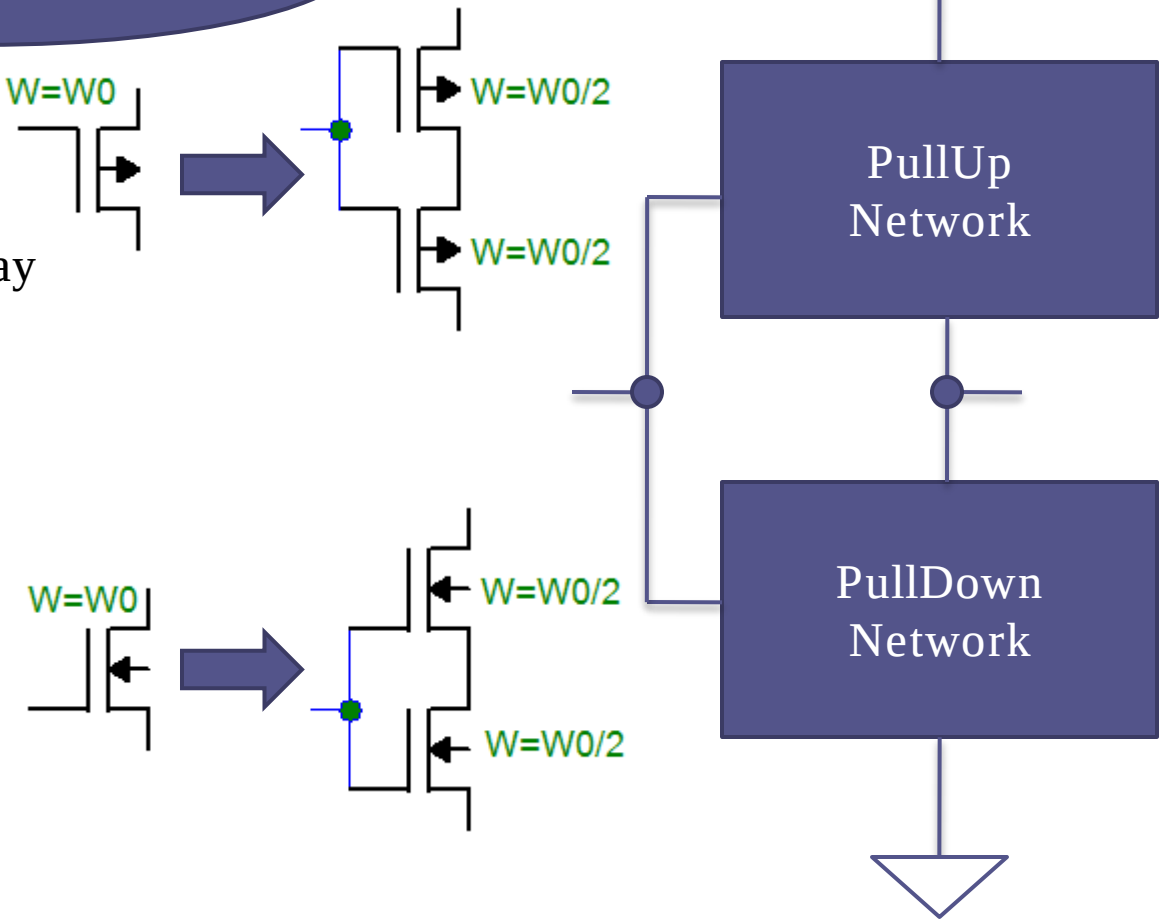
- ✓ State destructive (outputs are floating when in sleep mode)
- ✓ Need retention circuitry
- ✓ May be applicable for large digital blocks
- ✓Transistors with high V_{th} can be used



Schematic approaches for reducing the static power

Stack approach

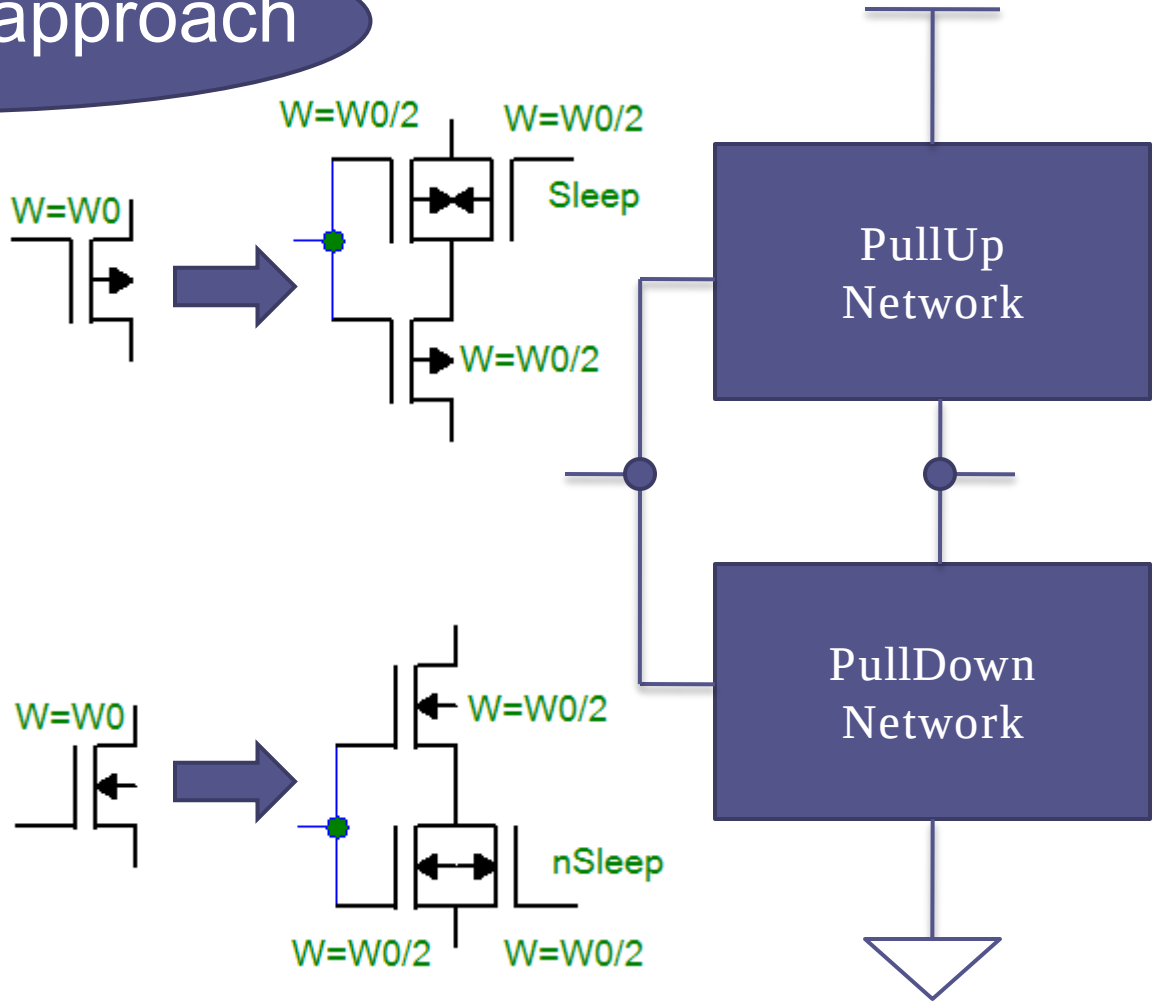
- ✓ State preserving
- ✓ Significantly reduces delay
- ✓ Reduced leakage due to reverse bias



Schematic approaches for reducing the static power

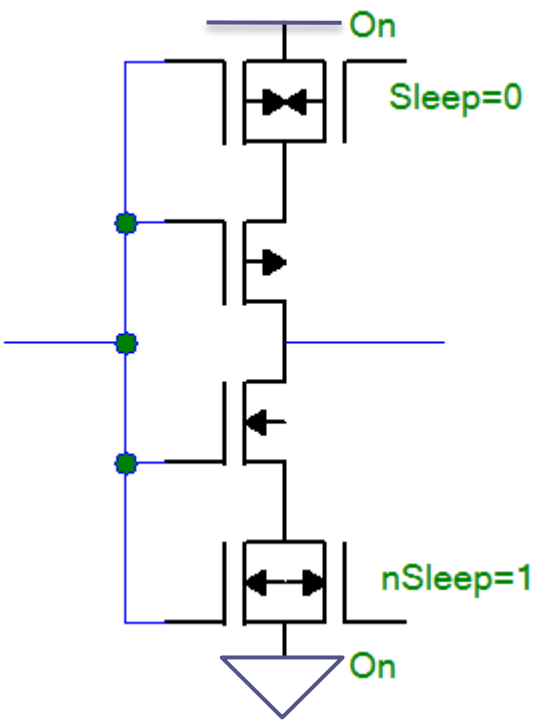
Sleepy stack approach

- ✓ State preserving
- ✓ Better delay vs. stack approach
- ✓ Reduced leakage due to reverse bias

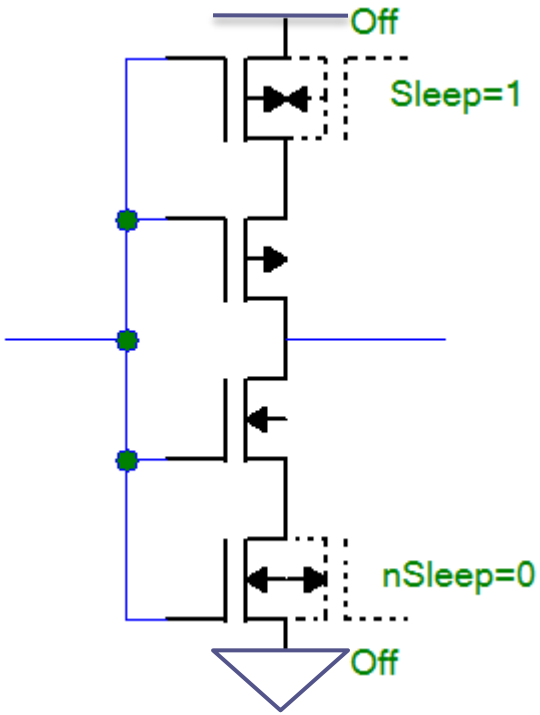


Schematic approaches for reducing the static power

Sleepy stack approach



Active mode – decreases the resistance path

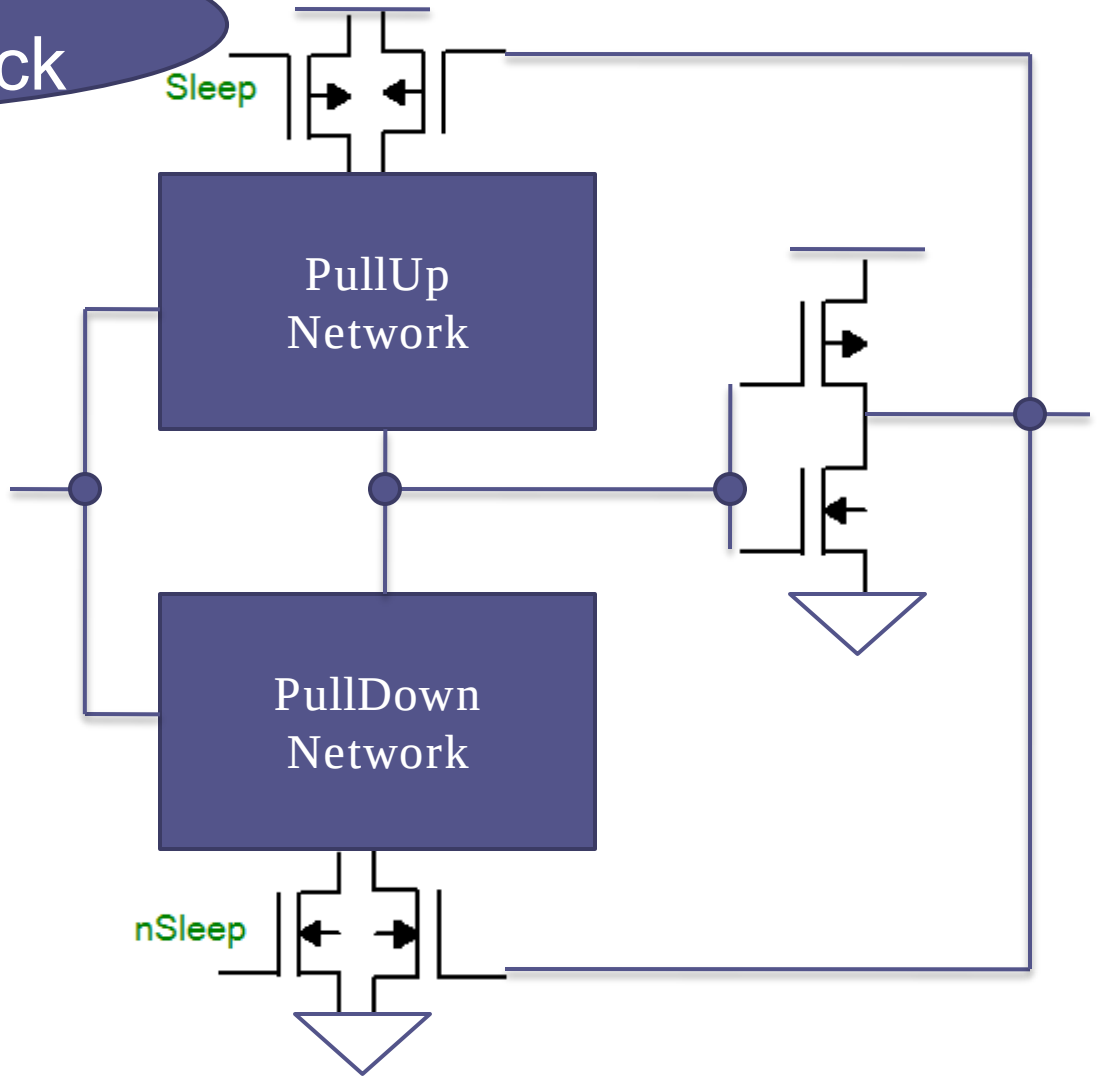


Sleep mode – like stack approach

Schematic approaches for reducing the static power

Approach with inverter in feedback

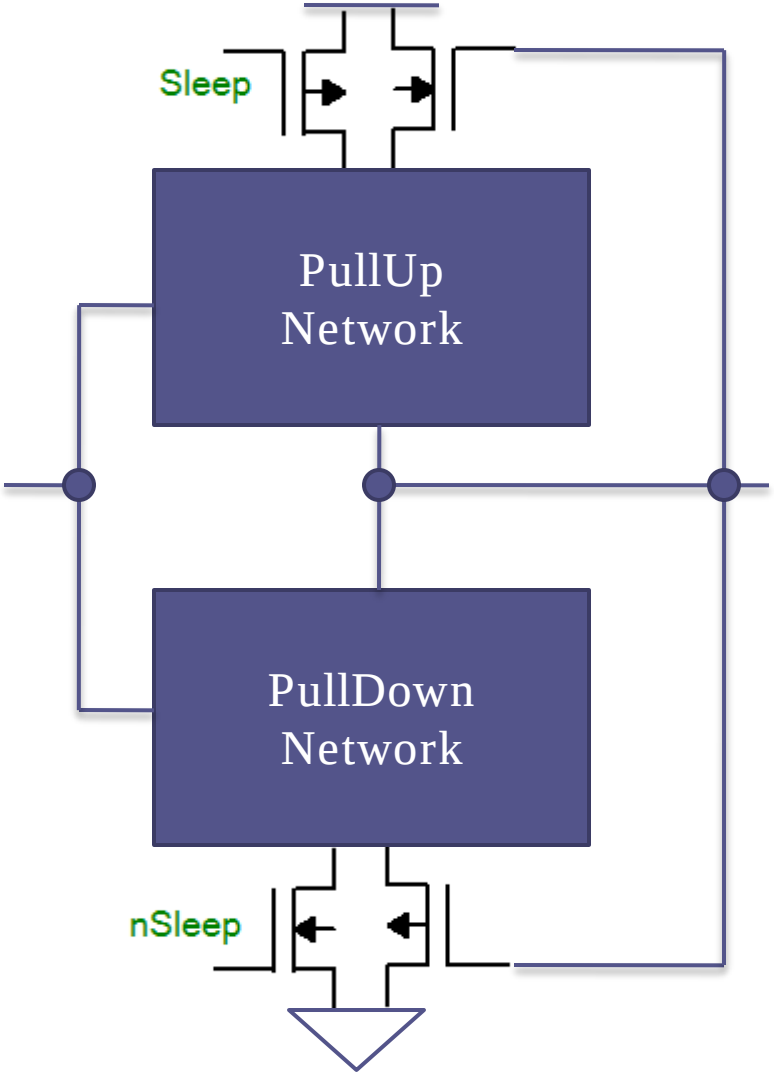
- ✓ State preserving
- ✓ Area overhead
- ✓ Additional leakage in inverter



Schematic approaches for reducing the static power

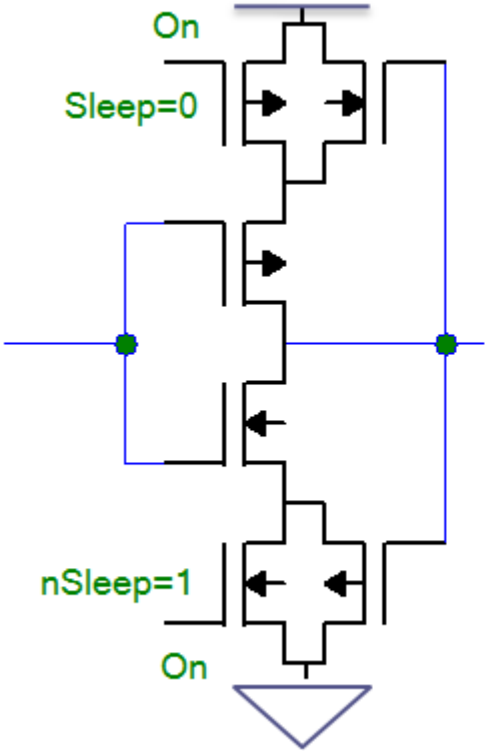
Sleepy keeper approach

- ✓ State preserving
- ✓ Less area overhead vs. sleep stack approach
- ✓ Minimal delay

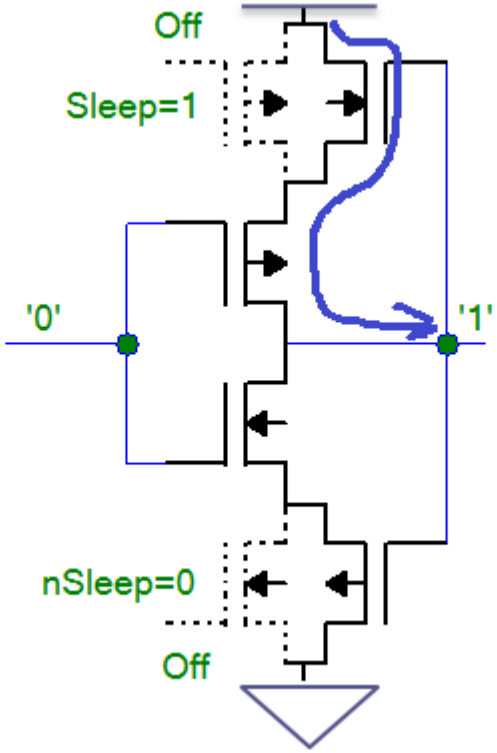


Schematic approaches for reducing the static power

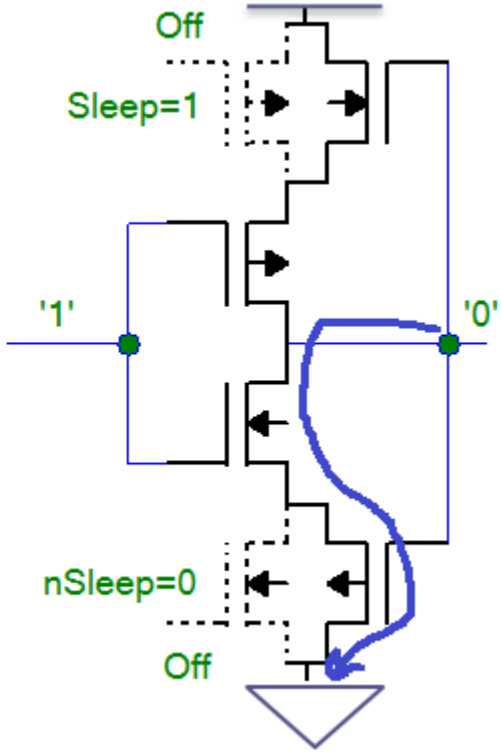
Sleepy keeper approach



Active mode:
sleep transistors are ON - reducing delay



NMOS is used to maintain ‘1’ in sleep mode

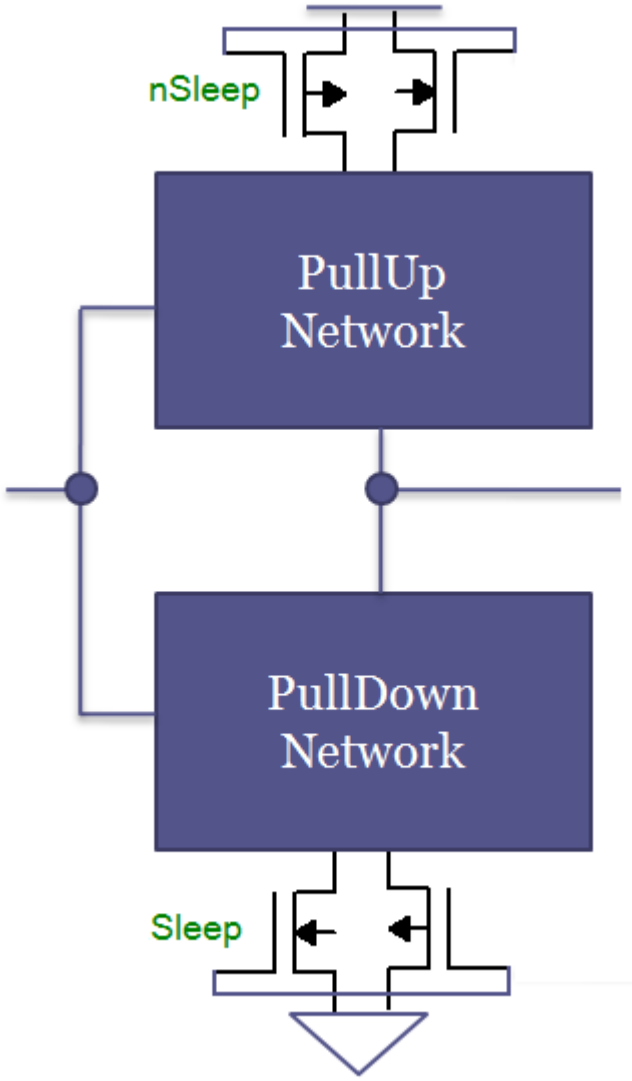


PMOS is used to maintain ‘0’ in sleep mode

Schematic approaches for reducing the static power

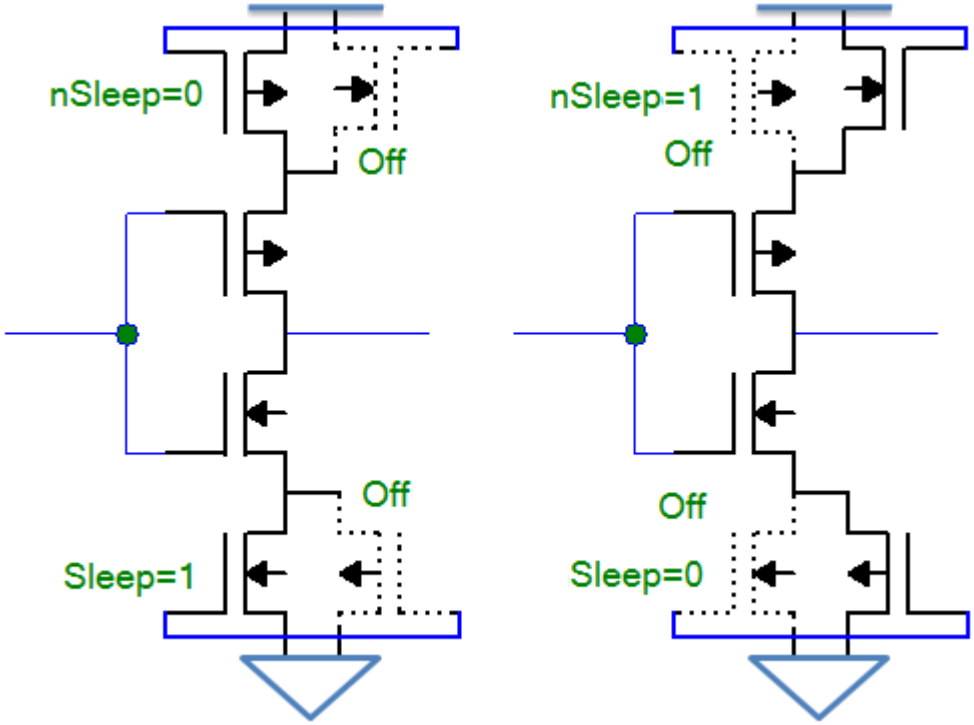
Dual sleep approach

- ✓ State-saving
- ✓ Very good delay values
- ✓ More static power reduction vs. sleepy keeper approach
- ✓ Proposed significant area reduction



Schematic approaches for reducing the static power

Dual sleep approach

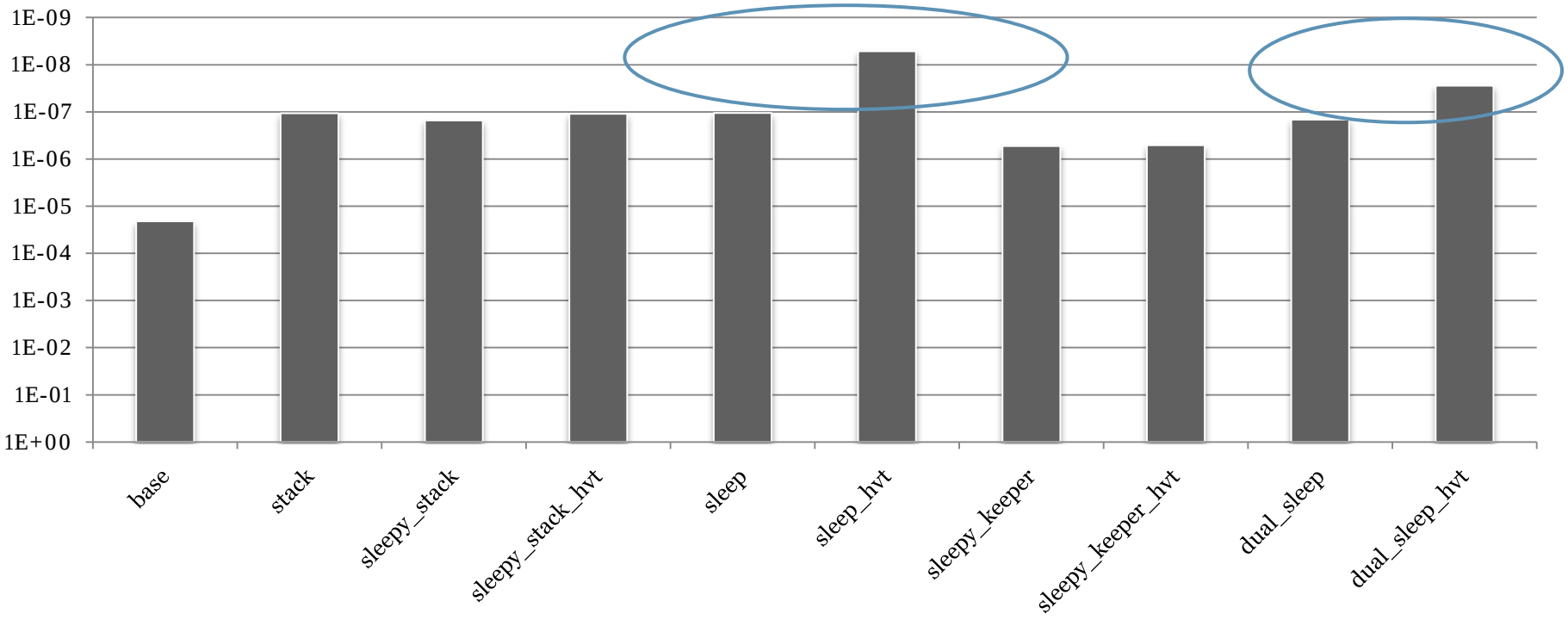


Active mode: normal device

PMOS is in series with NMOS

Results of modeling

Static power consumption of 4-bit adder realization for 90 nm technology, W



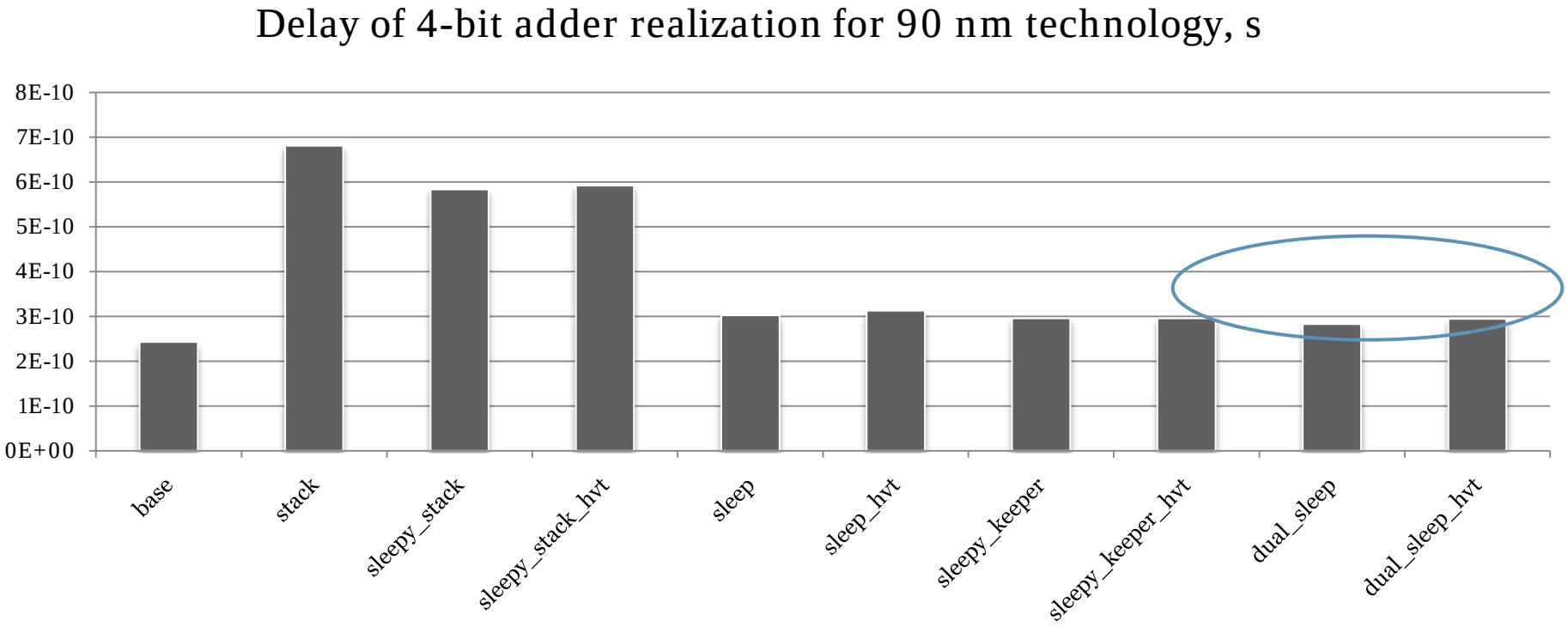
✓ Stack and sleepy_stack approaches results in roughly 2.5 order of magnitude leakage reduction

✓ Sleepy_keeper approach results in roughly 1.5 order of magnitude leakage reduction

✓ Sleep approach is the leader with 3.5 order

✓ Dual sleep approach (high-Vt) results 3.86X more reduction vs. stack approach and 19X more reduction vs. dual_sleep

Results of modeling

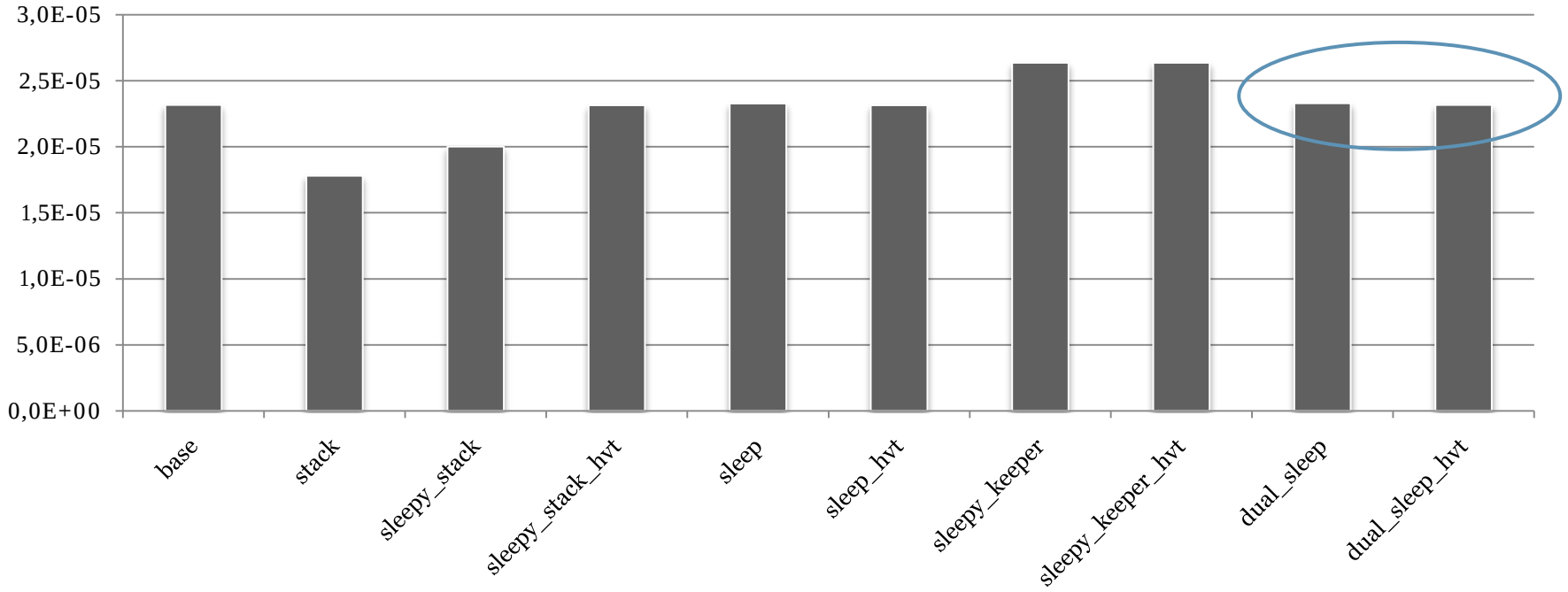


✓ Sleepy_stack and stack approaches have great delay penalty (up to 2.8X over base case for stack approach)

✓Sleep and sleepy_keeper approaches results in best delay over all methods (only 1.2X penalty for sleepy_keeper approach)

Results of modeling

Dynamic power consumption of 4-bit adder realization for 90 nm technology, W



✓ Stack approach consume 23% less dynamic power than the base circuitry but sleepy_keeper approach results in 14% more dynamic power

Results of modeling

Results for base logic element 4-bit adder

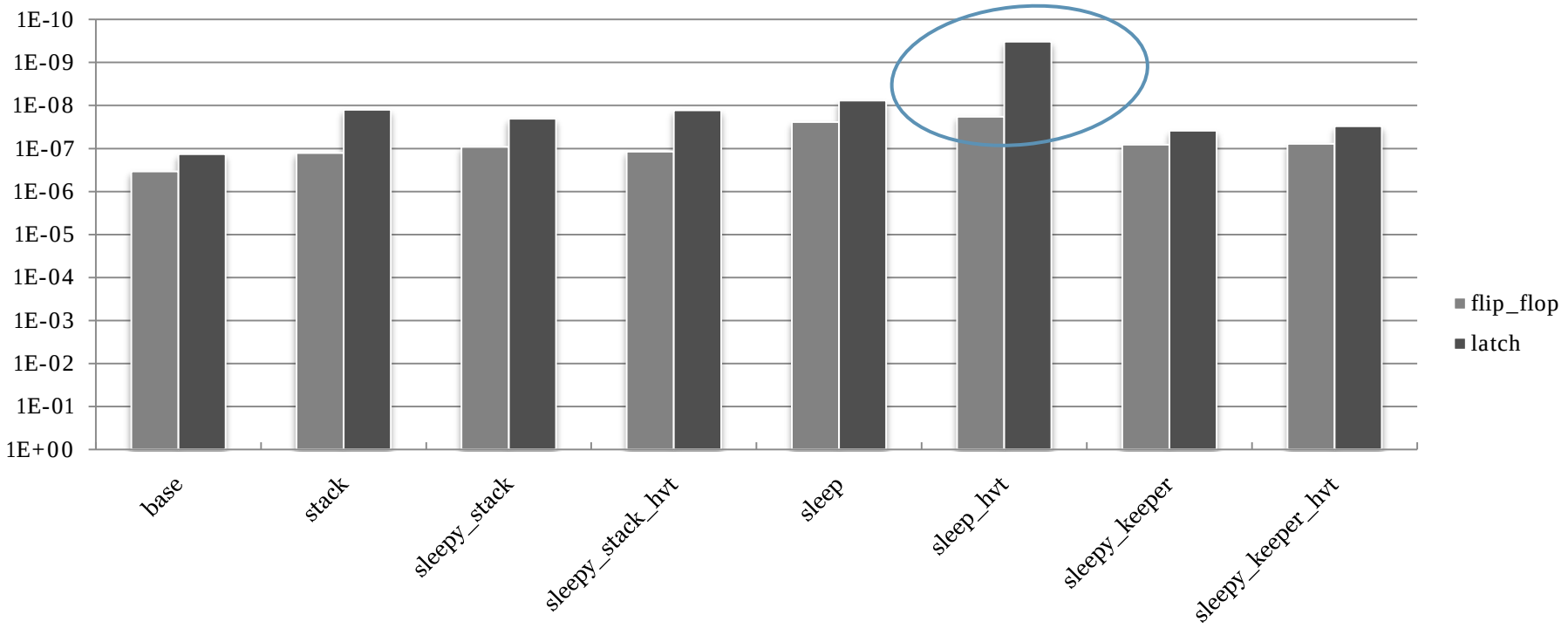
90nm	Static power, W	Dynamic power, W	Delay, s	Area
Stack	196X	0,8X	2.8X	1.35X
Sleep	199X	1X	1.2X	1.35X
Sleep (multi-Vth)	4044X	1X	1.3X	1.35X
Sleepy Stack	139X	0,9X	2.4X	2.87X
Sleepy Stack (multi-Vth)	199X	1X	2.4X	2.87X
Sleepy Keeper	40X	1,1X	1.2X	1.93X
Sleepy Keeper (multi-Vth)	41X	1,1X	1.2X	1.93X
Dual sleep	145X	1X	1.2X	?
Dual sleep (multi-Vth)	775X	1X	1.2X	?

Conclusions of modeling

- The novel dual sleep approach shows the best performance among the state-saving techniques
- Dual sleep approach also shows the delay values compared to the delay of sleepy_keeper approach and they are minimal for all state-saving techniques
- The minimal area overhead vs. sleepy_keeper approach in the case of many of the sequentially connected homogeneous circuits
- According to the analysis it's better for designers to use sleepy_keeper and dual sleep approaches
- Previous approaches are also effective in some cases, based upon the technology and design criteria

Results of modeling

Static power consumption of flip-flop and latch realization for 90 nm technology, W



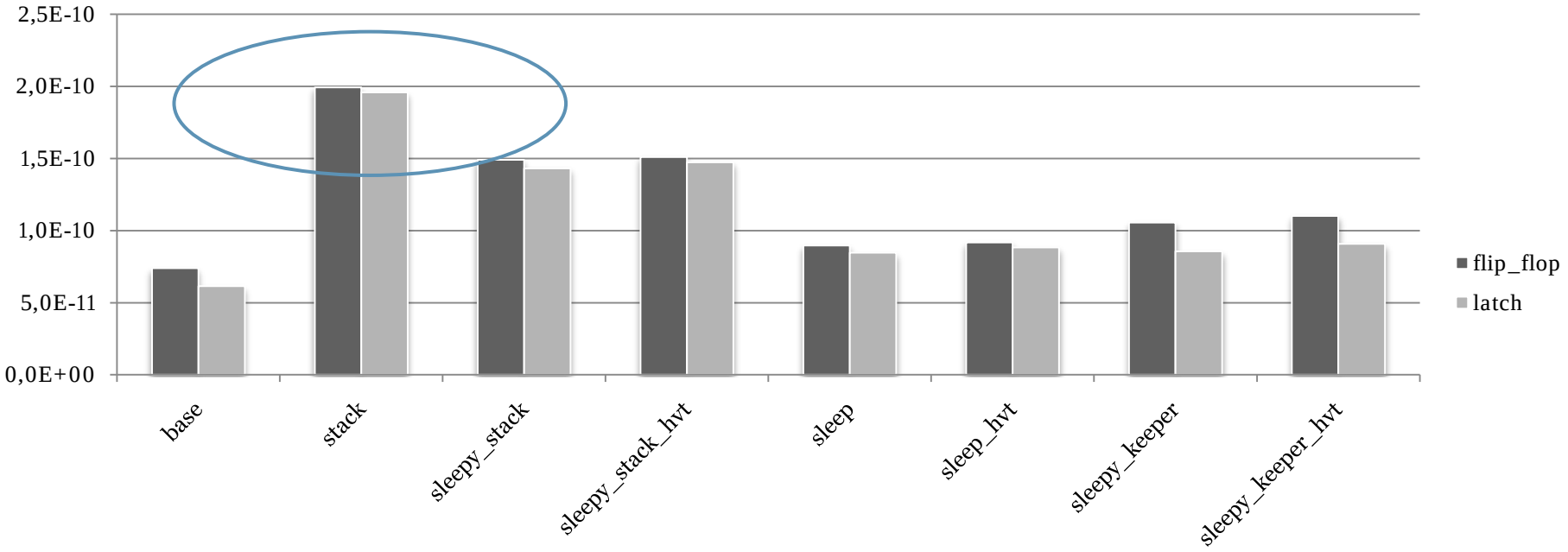
✓ Stack and sleepy_stack approaches using Multi V_{th} have 1 order of magnitude leakage reduction over the base case

✓ Sleepy_keeper approach results only 0.5 order of magnitude leakage reduction

✓ State-destructive sleep approach leads to the highest reduction using transistors with high threshold voltage: 2.1 order of magnitude

Results of modeling

Delay of flip-flop and latch realization for 90 nm technology, s

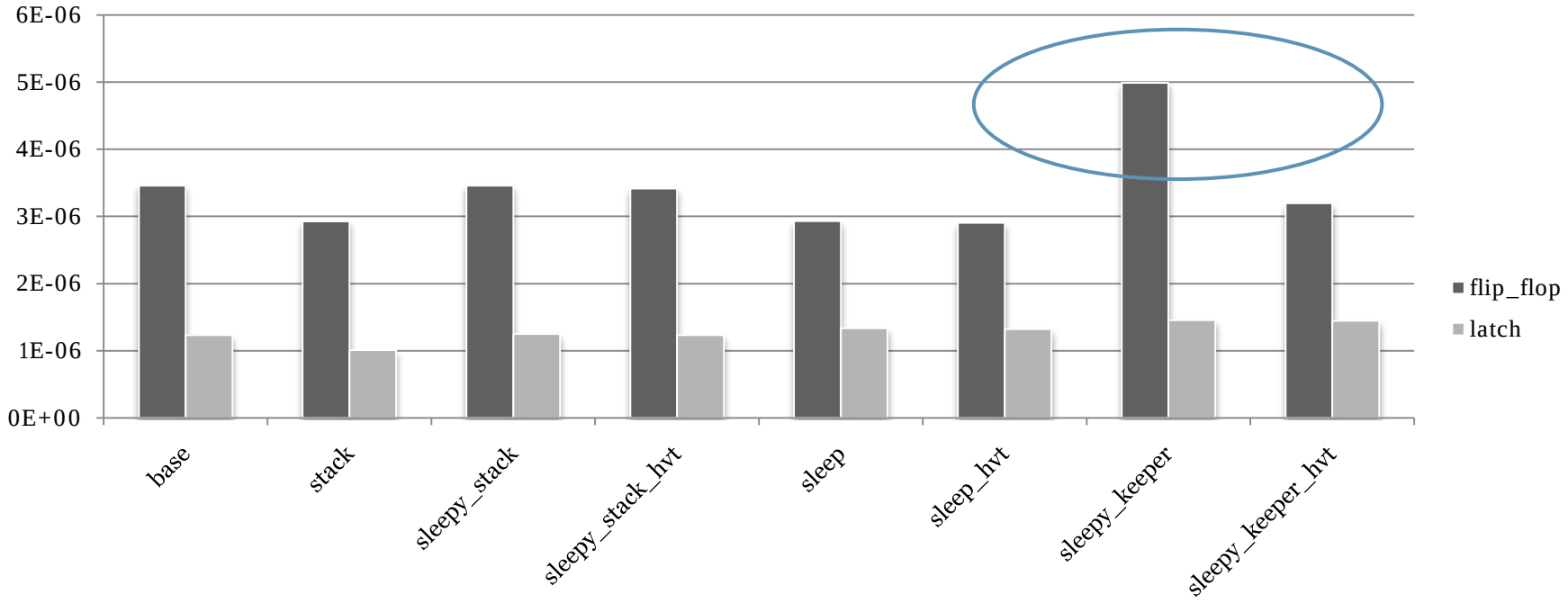


✓ Sleepy_stack and stack approaches have great delay penalty again (up to 2.7X over base case for stack approach)

✓Sleep and sleepy_keeper approaches results in best delay for latch over all methods (1.4X penalty for sleepy_keeper approach for latch)

Results of modeling

Dynamic power consumption of flip-flop and latch realization for 90 nm technology, W



✓ Sleepy_keeper approach consume 44% more dynamic power than the base circuitry for flip_flop

Conclusions of modeling

- All these methods of static power reduction can be applied to the trigger circuits
- They are not so efficient, as if we'll use them in sequential circuits

Suggestions for future work

- Analysis of usage dual sleep approach with trigger circuits (flip-flop, latch)

- Analysis of impact the threshold voltage and temperature variation on dependence of static power, dynamic power and delay using state-saving techniques

Thank you!